Maintenance Manual

ECE 492 - Spring 2019

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Abstract

This document details the technical (low-level) information for the Tractive System Voltage (TSV) subsystem within the LFEV 2019 Electric Car project.

Table of Contents

Introduction:

This document will lay out the new mechanical and electrical design of the battery packs and describe the design decisions that were made.

The TSV subsystem delivers the high voltage power for the Formula SAE hybrid electric vehicle. Each pack or accumulator container, numbered 1-2, supplies around 48 V through 14 LiFePO cells. These cells are monitored through the accumulator management system (AMS) which is comprised of a CellMan board, for monitoring individual cells, SegMan board, for monitoring one segment (7 battery cells); and PacMan, the computer of the pack. The cells within the packs and the packs themselves are connected in series to provide ~96 V.

Additional information of the TSV subsystem, such as bill of materials (BOM), schematics, hardware, mounting etc, some of which are detailed in this document, can be found in the LFEV website on the TSV page.

See: https://sites.lafayette.edu/motorsports/tsv/

Advanced Maintenance:

PacMan Firmware

The firmware of the PacMan will focus on determining the parameters state of charge of the cells, cell faults, under voltage, etc. These parameters can be configured using the pushbuttons and the LCD screen on the packs. The PacMan utilizes an Isolated Serial Peripheral Interface (ISO-SPI) to communicate with the SegMan, more details in the SegMan section, to actively balance the cells per segment. To achieve this, it will extract parameters from the SegMan such as cell voltage, discharge rate, and cell temperature. Using this information, the PacMan can determine when to continue charging a cell or when to stop charging a cell.

The PacMan controls the LCD touchscreen and its control buttons (UP, DOWN and ENTER) using an I2C communication protocol.

PacMan is able to trip the safety loop as a safety measure. Furthermore, it uses CAN communication to interface with SCADA. The communication firmware has been developed this semester, the active balancing firmware will be further developed next semester.

PackMan Hardware

The PacMan uses an ESP-WROOM-32 processor to store and make decisions about the state of the cells. The processor uses an external crystal clock source as a default CPU clock. The crystal clock is also connected to a PLL to generate ~160MHz. he PacMan is powered by the GLV battery. GLV power is sent to a DC-DC converter to step the 24 V signal to 3.3 V. The ESP has configurable low power management (Table 1).

The PacMan will control the high voltage LED indicator that lives on top of the pack. The HV+ and HV- signals are inputted to a DC-DC converter which will supply the necessary voltage to power the LED. The functionality of this LED is important to classify the packs as removable packs.

Both safety loop signals (SL1 and SL2) will be inputs to the PacMan. This way, if there is an issue with the pack then the PacMan can intercept the safety loop relay.

Power mode	Description			Power consumption
Active (RF working)	Wi-Fi Tx packet			Please refer to Table 14 for details.
	Wi-Fi/BT Tx packet			
	Wi-Fi/BT Rx and listening			
Modem-sleep	The CPU is powered on.	240 MHz *	Dual-core chip(s)	30 mA ~ 68 mA
			Single-core chip(s)	N/A
		160 MHz *	Dual-core chip(s)	27 mA ~ 44 mA
			Single-core chip(s)	27 mA ~ 34 mA
		Normal speed: 80 MHz	Dual-core chip(s)	20 mA ~ 31 mA
			Single-core chip(s)	20 mA ~ 25 mA
Light-sleep	-			0.8 mA
Deep-sleep	The ULP co-processor is powered on.			150 μA
	ULP sensor-monitored pattern			100 μA @1% duty
	RTC timer + RTC memory			10 μA
Hibernation	RTC timer only			5 μA
Power off	CHIP_PU is set to low level, the chip is powered off.			0.1 μA

Table 1: ESP32 Low-Power Management Modes

SegMan

The SegMan will use ISO-SPI protocol to communicate with the PacMan. The SegMan itself does not have a processor but does have digital logic through the LTC6804-1. This digital logic will allow the SegMan to store relevant information about the expected cell performance (provided by the PacMan) in memory. Then, the SegMan will use the pin Sn to transmit a signal to enable/disable discharging. Table 2 shows how the LTC6804 indexes through the cells to transmit information.

The SegMan is powered by a segment of cells (7 cells / ~24V) by directly connecting to the positive and negative terminals of a segment. This connection needs to be fused to avoid overpowering the LTC6804-1. The ideal location of the SegMan is right on the segment divider facing one segment of cells. The SegMan will also have the ISO-SPI chip LTC6820 which is rated at 3.3V for communication. The segment voltage on the SegMan needs to go through a DC-DC converter to get 3.3 V.

For more information about the SegMan, refer to the SegMan block diagram and the high-level wiring diagram at the end of this document.

Table 36. Configuration Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	SWTRD	ADCOPT
CFGR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 37. Cell Voltage Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVAR0	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVAR1	RD	C1V[15]	C1V[14]	C1V[13]	C1V[12]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVAR2	RD	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	RD	C2V[15]	C2V[14]	C2V[13]	C2V[12]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR4	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVAR5	RD	C3V[15]	C3V[14]	C3V[13]	C3V[12]	C3V[11]	C3V[10]	C3V[9]	C3V[8]

Table 38. Cell Voltage Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVBR0	RD	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
CVBR1	RD	C4V[15]	C4V[14]	C4V[13]	C4V[12]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVBR2	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVBR3	RD	C5V[15]	C5V[14]	C5V[13]	C5V[12]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVBR4	RD	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR5	RD	C6V[15]	C6V[14]	C6V[13]	C6V[12]	C6V[11]	C6V[10]	C6V[9]	C6V[8]

Table 39. Cell Voltage Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVCR0	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVCR1	RD	C7V[15]	C7V[14]	C7V[13]	C7V[12]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVCR2	RD	C8V[7]	C8V[6]	C8V[5]	C8V[4]	C8V[3]	C8V[2]	C8V[1]	C8V[0]
CVCR3	RD	C8V[15]	C8V[14]	C8V[13]	C8V[12]	C8V[11]	C8V[10]	C8V[9]	C8V[8]
CVCR4	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVCR5	RD	C9V[15]	C9V[14]	C9V[13]	C9V[12]	C9V[11]	C9V[10]	C9V[9]	C9V[8]

Table 40. Cell Voltage Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVDR0	RD	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVDR1	RD	C10V[15]	C10V[14]	C10V[13]	C10V[12]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVDR2	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVDR3	RD	C11V[15]	C11V[14]	C11V[13]	C11V[12]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVDR4	RD	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]
CVDR5	RD	C12V[15]	C12V[14]	C12V[13]	C12V[12]	C12V[11]	C12V[10]	C12V[9]	C12V[8]

Table 2: SegMan Cell Assignment by Group

CellMan

The CellMan is a small board that receives its power from the cell it is monitoring. The four corners of the CellMan have screw holes in order to directly connect to the busbars on top of a cell. Make sure to connect it to the farthest screw terminal on the busbar

The CellMan has a chip LTC8584 which receives information from the SegMan on whether to discharge a cell or not. When discharging, the CellMan will intercept the incoming current and divert it back to the rest of the cells (refer to the high-level wiring diagram) to actively balance the cells.

For more information about the CellMan refer to the CellMan wiring diagram, high-level pack wiring diagram or the CellMan block diagram (links on page 7).

Cells

Dead Cells

If a Cell reads <2V, attempt charging the individual cell to 3.4V. If it maintains this charge, you are good to go. If it can not maintain a charge, you need to replace the cell.

Pack

Safety Loop

If the safety loop is not closing as expected, check the 8 pin connector and make sure that all the wires are secured.

Charging

If a pack is unable to charge, check the continuity from the charging port to the connectors that insert into the SegMan.

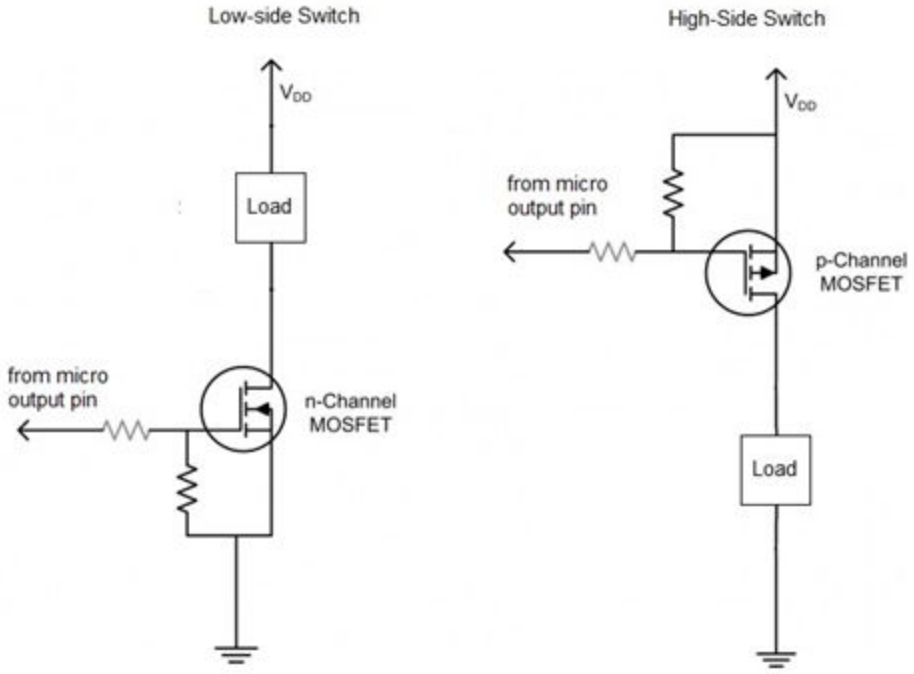
Errata

CellMan

1. The 4-pin connector (J1) should be changed to two 2-pin connectors. This is to separate the high current Vseg + and Vseg - connection with the data out and data in (Cn and Sn respectively).
2. Add a current sensor in the PCB to measure the charging current
3. Position the connectors so that they are not too close to the other connectors on the PCB

SegMan

1. Q1 is an N-channel Mosfet and it is currently configured as a high side switch. This will not work. Configure this a low side switch to drive the Charge Relay.



2. The charge circuit needs to be fused. Add 20 A fusing for J8 on both Chrg+ and Chrg-.
3. There is no way for PacMan to know when the Charger is plugged into the Charge Port. See prior PacMan Charge port detection implementation.
    a. Detect shorted jumper in charger from extra pins in charge port.
    b. Be able to control the Charge Relay K1 from the Pack User interface.

4. The Charge Relay K1 does not fit in the SegMan PCB
    a. Find another 20 A DPDT switch relay that fits in the board
    b. Build a panel mount scheme for the current relay and use wires to connect to the SegMan PCB

PacMan

Mechanical Block Diagram:

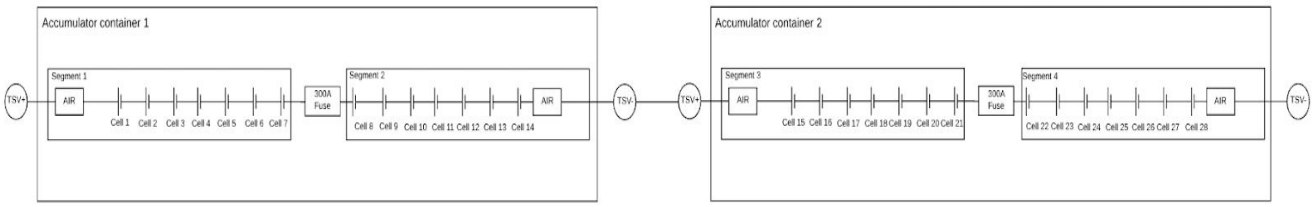


Figure 1: Block diagram of the accumulators in the car

Electrical Block Diagram Links

PacMan

https://sites.lafayette.edu/motorsports/files/2019/04/pacman-block-diagram.jpg

SegMan

https://sites.lafayette.edu/motorsports/files/2018/12/SegMan_block_diagram-1.pdf

CellMan

https://sites.lafayette.edu/motorsports/files/2018/11/CellMan_Block_Diagram.pdf

Wiring Schematic Links

CellMan

https://sites.lafayette.edu/motorsports/files/2018/11/CellMan-Schematic.pdf

SegMan

https://sites.lafayette.edu/motorsports/files/2019/03/SegMan_sch-2.pdf

PacMan

https://sites.lafayette.edu/motorsports/files/2019/03/pacman_schematic.pdf

Pack (internal pack wiring diagram)

https://sites.lafayette.edu/motorsports/files/2018/11/Electrical-wiring-diagram-TSV.pdf

BOM Links

Pack BOM

https://sites.lafayette.edu/motorsports/files/2018/12/2019-Accumulator-BOM.xlsx

CellMan BOM

https://sites.lafayette.edu/motorsports/files/2019/04/CellMan_BOM.csv

SegMan BOM

https://sites.lafayette.edu/motorsports/files/2019/04/SegMan_BOM.csv

PacMan BOM

https://sites.lafayette.edu/motorsports/files/2019/05/PacMan_BOM.xlsx

Mechanical Drawing

https://sites.lafayette.edu/motorsports/files/2018/12/Battery-pack-total-assembly.zip