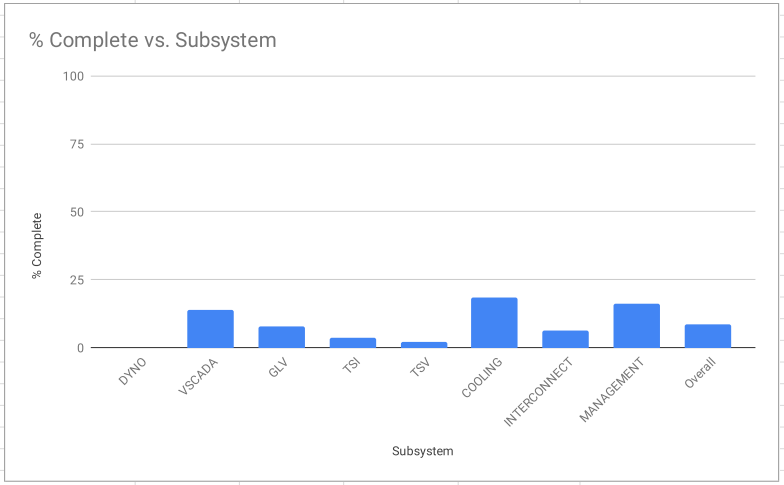
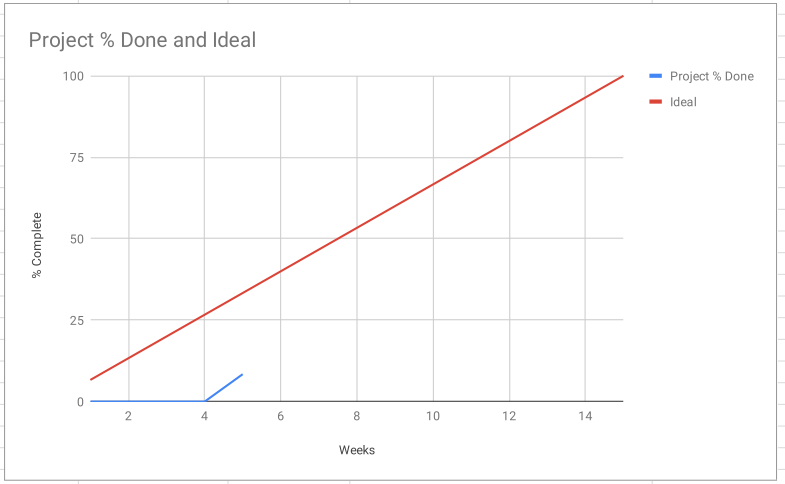
Subsystem	% Complete	Total # Tasks	# Tasks Complete	# Tasks Remaining
DYNO	0	27	0	27
VSCADA	13.95348837	43	6	37
GLV	7.936507937	63	5	58
TSI	3.571428571	56	2	54
TSV	2.127659574	47	1	46
COOLING	18.51851852	27	5	22
INTERCONNECT	6.12244898	49	3	46
MANAGEMENT	16.07142857	56	9	47
Overall	8.423913043	368	31	337

PROJECT % COMPLETE: 8.423913043

Weeks	Project % Done	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	8.423913043	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100



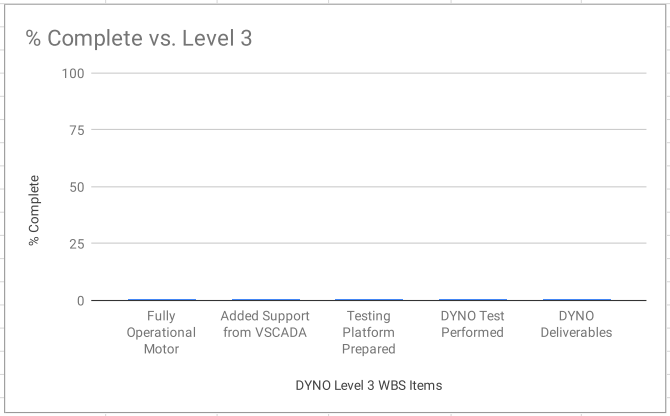


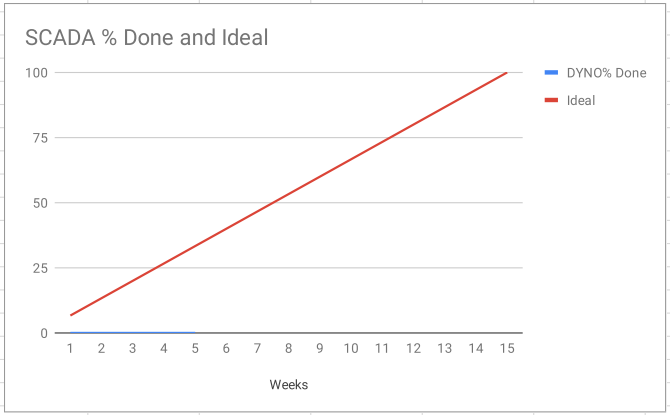
DYNO Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complete	# Tasks Remaining
Fully Operational Motor	0	4	0	4
Added Support from VSCADA	0	6	0	6
Testing Platform Prepared	0	7	0	7
DYNO Test Performed	0	4	0	4
DYNO Deliverables	0	6	0	6
Total	0	27	0	27

DYNO% COMPLETE	0

WBS Items comp	Description
N/A	N/A

Weeks	DYNO% Done	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	0	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100



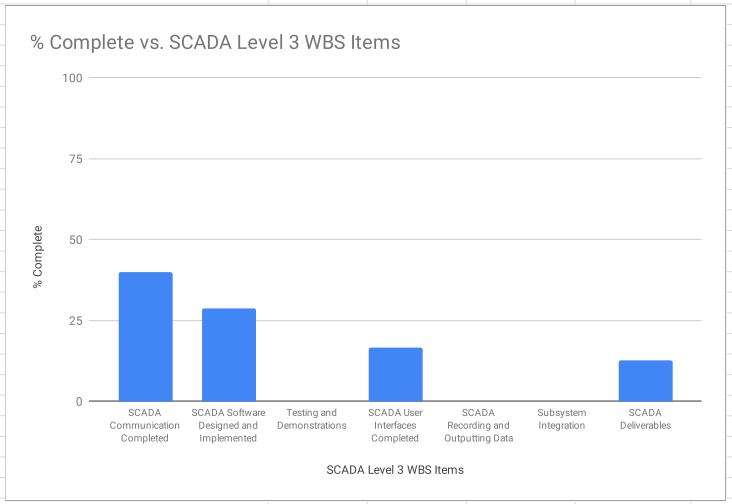


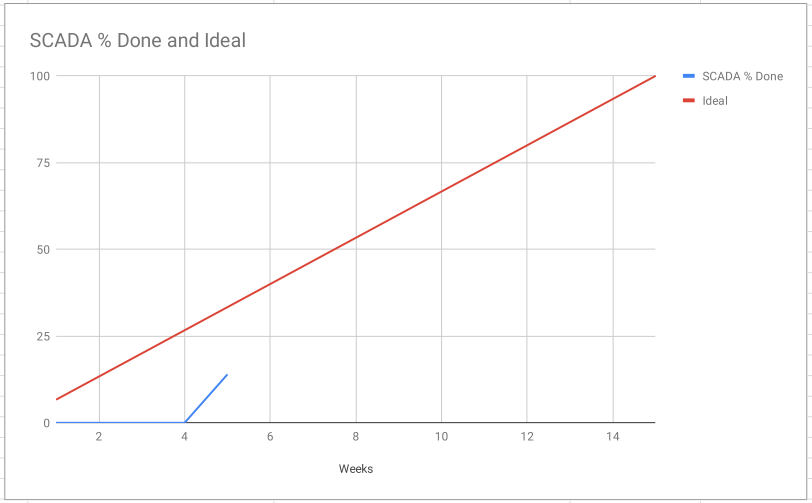
SCADA Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complete	# Tasks Remaining
SCADA Communication Completed	40	5	2	3
SCADA Software Designed and Implemented	28.57142857	7	2	5
Testing and Demonstrations	0	7	0	7
SCADA User Interfaces Completed	16.66666667	6	1	5
SCADA Recording and Outputting Data	0	5	0	5
Subsystem Integration	0	5	0	5
SCADA Deliverables	12.5	8	1	7
Total	13.95348837	43	6	37

WBS Item Completed	Description
SCADA.1.1	Setup CAN Network
SCADA.1.2	Setup Database Handler and Fill with Dummy Data
SCADA.2.1	Software Block Diagram Delivered
SCADA.2.6	Testing Plan Delivered
SCADA.4.2	Back Display Designed and Delivered
SCADA.7.2	PDR Delivered to Management

SCADA % COMPLETE	13.95348837

Weeks	SCADA % Done	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	13.95348837	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100



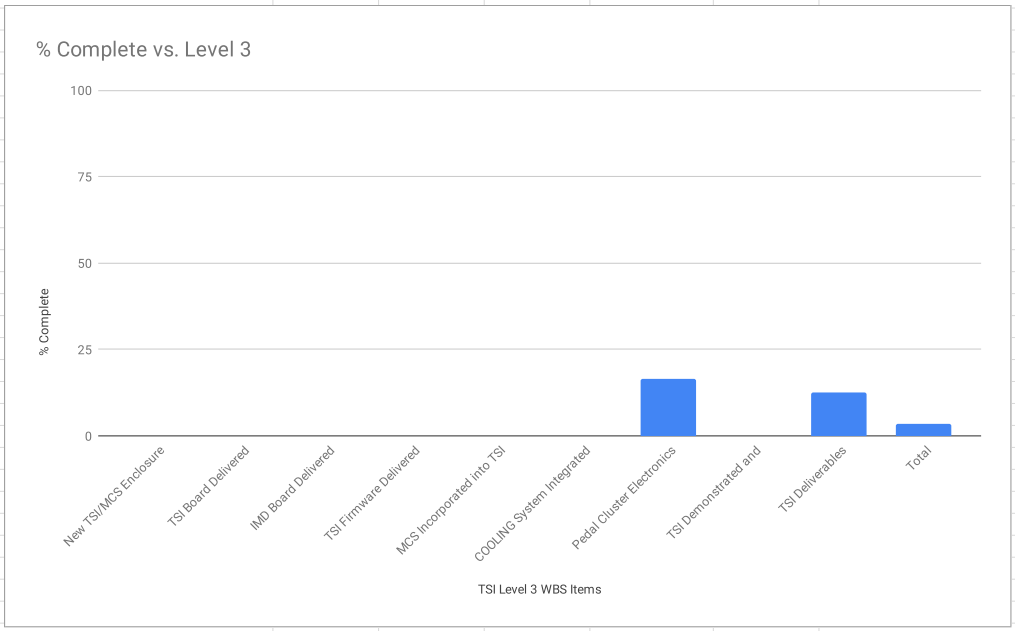


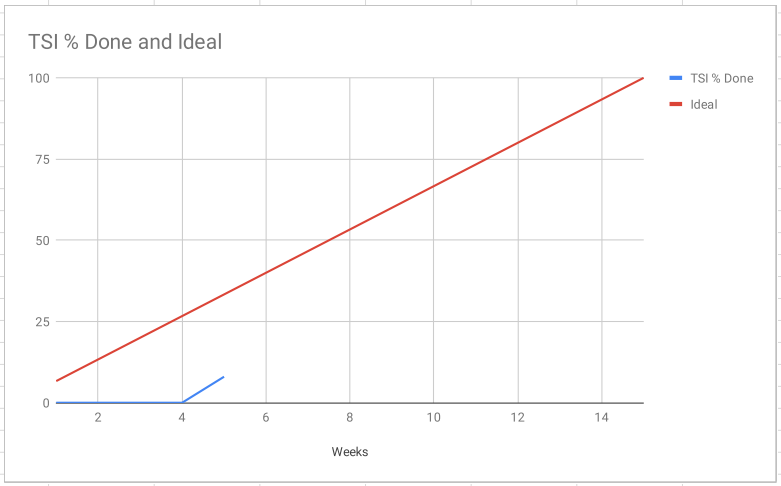
TSI Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complet	# Tasks Remaining
New TSI/MCS Enclosure Built and Delivered	0	3	0	3
TSI Board Delivered	0	7	0	7
IMD Board Delivered	0	5	0	5
TSI Firmware Delivered	0	12	0	12
MCS Incorporated into TSI Enclosure	0	5	0	5
COOLING System Integrated into TSI	0	4	0	4
Pedal Cluster Electronics	16.66666667	6	1	5
TSI Demonstrated and Accepted	0	7	0	7
TSI Deliverables	12.5	8	1	7
Total	3.50877193	57	2	55

WBS Items completed	Description
TSI.7.1	Verify and correct 2018 Block and Wiring Diagram
TSI.9.1	PDR Delivered to MGMT

TSI % COMPLETE	3.508771

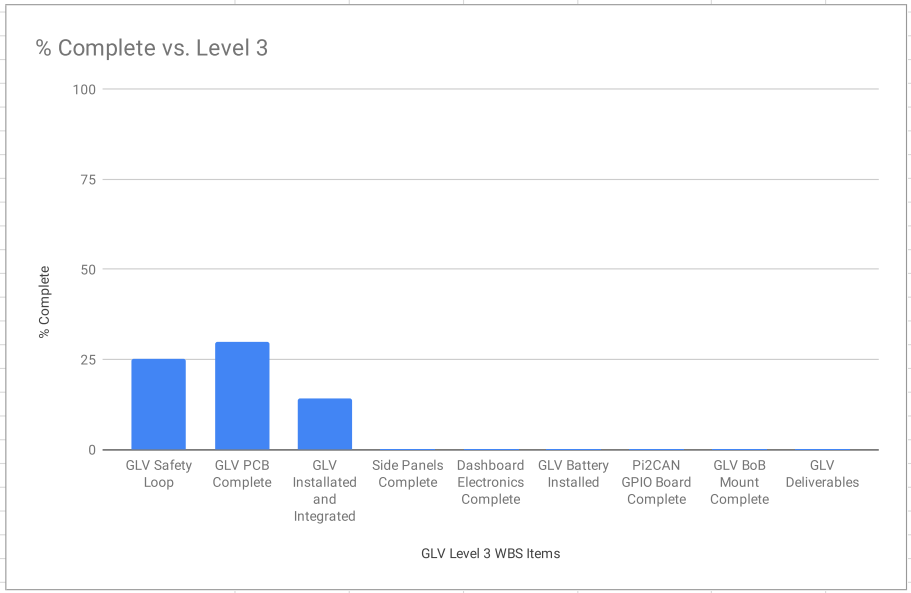
Weeks	TSI % Done	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	8	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100

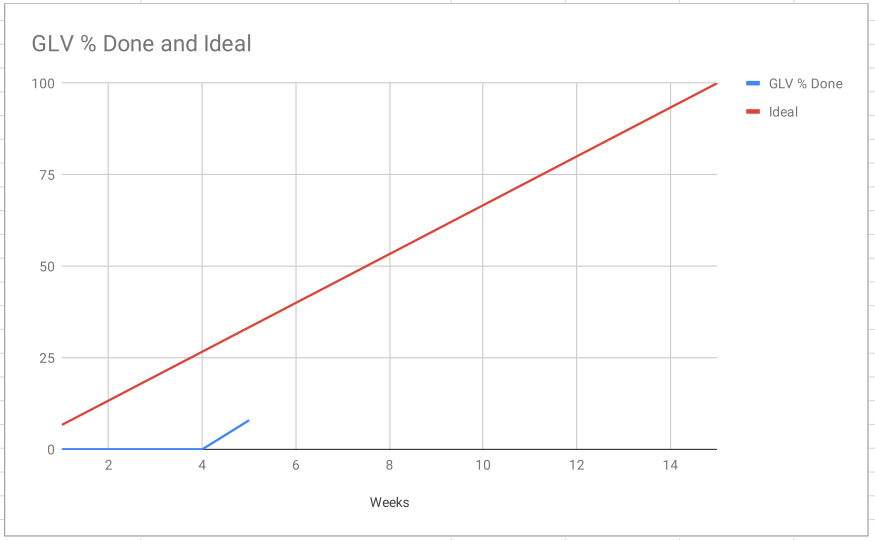




GLV Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complet	# Tasks Remaining
GLV Safety Loop	25	4	1	3
GLV PCB Complete	30	10	3	7
GLV Installated and Integrated	14.28571429	7	1	6
Side Panels Complete	0	8	0	8
Dashboard Electronics Complete	0	3	0	3
GLV Battery Installed	0	4	0	4
Pi2CAN GPIO Board Complete	0	9	0	9
GLV BoB Mount Complete	0	10	0	10
GLV Deliverables	0	8	0	8
Total	7.936507937	63	5	58

WBS Items completed	Description	Weeks	GLV % Done	Ideal
GLV.1.1	Safety Loop Block Diagram Completed	1	0	6.666666667
GLV.2.1	GLV Block Diagram completed	2	0	13.33333333
GLV.2.2	GLC Circuit Schematic Delivered	3	0	20
GLV.2.4	GLV Board BOM Approved	4	0	26.66666667
GLV.3.1	GLV Enclosure Mechanical Drawing Delivered	5	7.936507937	33.33333333
		6		40
		7		46.66666667
		8		53.33333333
		9		60
		10		66.66666667
		11		73.33333333
GLV % COMPLETE	7.936507937	12		80
		13		86.66666667
		14		93.33333333
		15		100



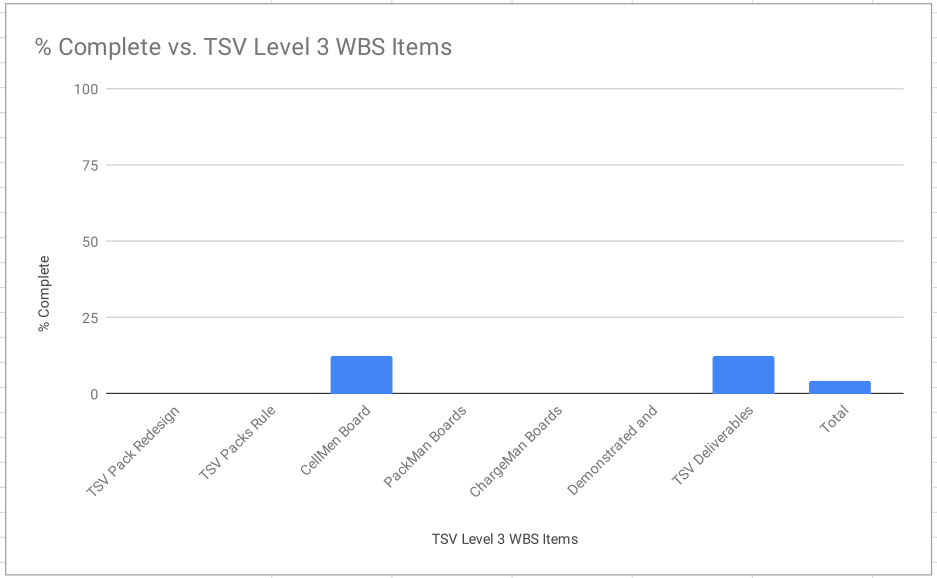


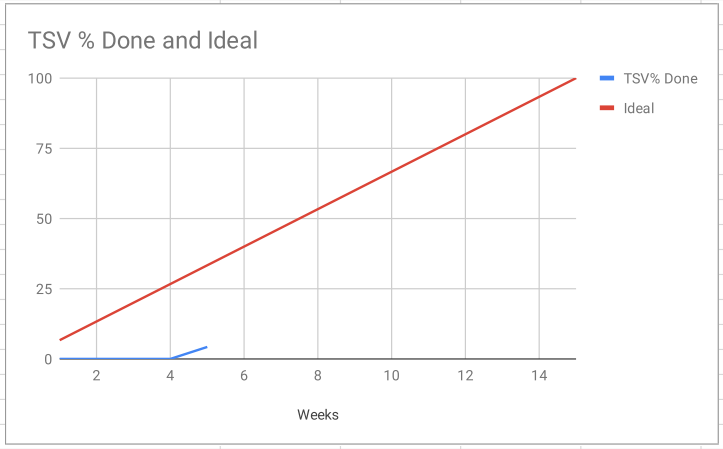
TSV Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complet	# Tasks Remaining
TSV Pack Redesign Delivered	0	8	0	8
TSV Packs Rule Compliance	0	2	0	2
CellMen Board Redesign Delivered	12.5	8	1	7
PackMan Boards Delivered	0	7	0	7
ChargeMan Boards Delivered	0	7	0	7
Demonstrated and Accepted	0	7	0	7
TSV Deliverables	12.5	8	1	7
Total	4.255319149	47	2	45

WBS Item Completed	Description
TSV.3.1	CellMen Block Diagram Delivered
TSV.7.1	PDR Delivered to Management

TSV% COMPLETE	4.255319

Weeks	TSV% Done	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	4.255319149	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100

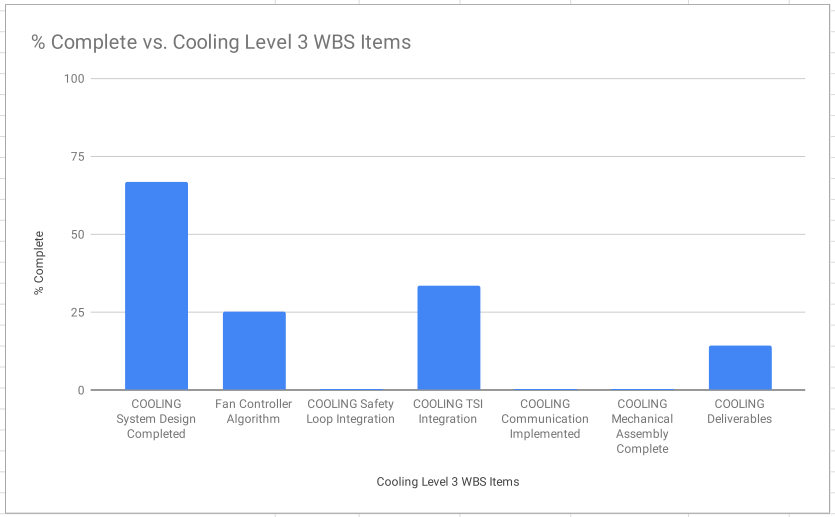




Cooling Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complete	# Tasks Remaining
COOLING System Design Completed	66.66666667	3	2	1
Fan Controller Algorithm	25	4	1	3
COOLING Safety Loop Integration	0	2	0	2
COOLING TSI Integration	33.33333333	3	1	2
COOLING Communication Implemented	0	4	0	4
COOLING Mechanical Assembly Complete	0	4	0	4
COOLING Deliverables	14.28571429	7	1	6
Total	18.51851852	27	5	22

WBS Item Completed	Description
COOLING.1.2	Block Diagram of Cooling System Delivered and Approved
COOLING.1.3	Electrical Schematic Delivered and Approved
COOLING.2.2	Controller Testing Plan Submitted
COOLING.4.1	Integration Plan for Cooling-TSI Submitted
COOLING.7.1	PDR Delivered to Management
COOLING % COMPLETE	18.51851852

Weeks	COOLING % Done	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	18.51851852	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100

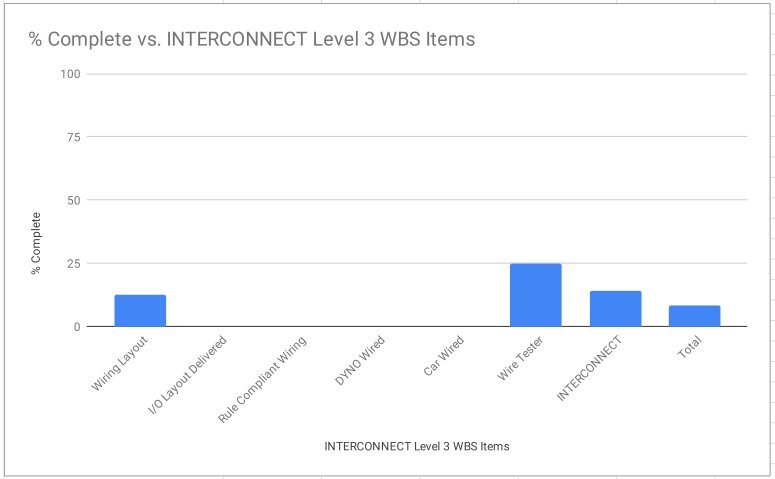


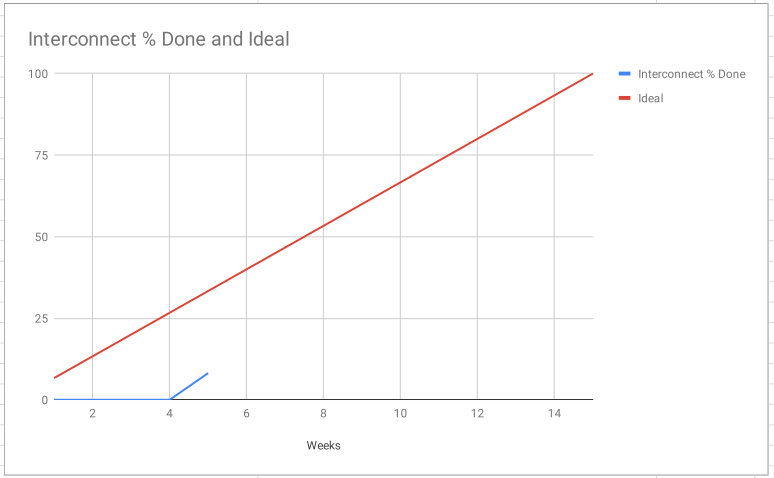
INTERCONNECT Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complet	# Tasks Remaining
Wiring Layout Delivered	12.5	8	1	7
I/O Layout Delivered	0	8	0	8
Rule Compliant Wiring	0	8	0	8
DYNO Wired	0	5	0	5
Car Wired	0	5	0	5
Wire Tester Constructed	25	8	2	6
INTERCONNECT Deliverables	14.28571429	7	1	6
Total	8.163265306	49	4	45

WBS Item Completed	Description
INTER.1.3	Incorporation of Previous Errata in Diagram
INTER.6.3	Wire Tester Prototype Circuit Built and Tested on Breadboard
INTER.6.4	Wire Tester Firmware Written and Tested on Breadboard Circuit
INTER.7.2	PDR Delivered to Management

INTERCONNECT% COMPLETE	8.163265306

Weeks	Interconnect % D	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	8.163265306	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100





Management Level 3 WBS Items	% Complete	Total # Tasks	# Tasks Complet	# Tasks Remaining
Preliminary Design Report (PDR) Complete	100	9	9	0
CDR Complete	0	5	0	5
Acceptance Test Plan (ATP) Complete	0	7	0	7
Final Presentation	0	5	0	5
Project Poster	0	3	0	3
Software Documentation	0	4	0	4
Paperwork	0	15	0	15
Communication	25	4	1	3
Purchasing Reports and BOM	0	4	0	4
Total	17.85714286	56	10	46

WBS Item Completed	Description
M.1.1	Budget Approved
M.1.2	Each Subsystem PDR Approved
M.1.3	PDR Maintainability Plan Approved
M.1.4	Overall Acceptance Strategy Delivered
M.1.5	Work Breakdown Structure Proposed
M.1.6	Task / Requirement Delegation Approved
M.1.7	Meeting Minutes Delivered
M.1.8	PDR Presentation Delivered
M.1.9	PDR Delivered
Management % Complete	17.85714286

Weeks	Management % D	Ideal
1	0	6.666666667
2	0	13.33333333
3	0	20
4	0	26.66666667
5	17.85714286	33.33333333
6		40
7		46.66666667
8		53.33333333
9		60
10		66.66666667
11		73.33333333
12		80
13		86.66666667
14		93.33333333
15		100