To: LFEV-ESCM Team

From: Drew Jeffrey

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Subject: PacMan Breakout Board Errata Memo

Abstract:

The PacMan Breakout Board is designed to allow the TS-8160-4200 SBC to operate system relays, provide isolation between high voltage and low voltage circuits, and allow measurement of pack level current and temperature readings. Because the PacMan Breakout Board ties together all the components of the battery pack, it design was finalized late in the development cycle in order to ensure the rest of the systems it would be interacting with were finalized. As such, the current PacMan Breakout Board layout has some minor errors in it which can be fixed in a second spin of the PCB. This document list the encountered errors and recommendations as to how they can be fixed in future versions of the board. Some of these changes have already been fixed in the DxDesigner or PADS layouts since the writing of this document.

Silkscreen Errors:

There were many issues with silkscreen in revision 1 of the PacMan BoB. The first set of errors were with regards to the Shrouded Locking Pin Headers covering many parts of the silkscreen since they extend beyond the parameter of the pin header holes due to the extra plastic they contain for the locking. In particular, the "Made in USA" lettering is greatly obscured by the ADC header. There are other cases where the components obscure the silkscreen, so it is suggested that the current populated board be reviewed before sending it for manufacturing to see if any silkscreened letters should be moved.

-Diode D4 currently does not have a polarity indicator. This should be added before revision 2 of the BoB is sent out for production.

-The 2 pin header decal in PADS switches pins 1 and 2. Due to this error, each pair of connections into a 2-pin header decale are flipped.

-J8: "SHUNT-" and "SHUNT+" should be flipped

-J9: “G” and “5V” should be flipped and Pin 1 (square pad) should be on the left side

-J11: “DET1” and “DET2” should be flipped.

-J12: “C RLY1-” and “C RLY1+” should be flipped

-J13: “C RLY2-” and “C RLY2+” should be flipped

-J15: “RS-485-” and “RS-485+” should be flipped

-J16: “CHRG NEG” and “CHRG POS” should be flipped

-J17: “SLOOP_OUT” and “SLOOP_IN” should be flipped

-J19: “FAN-” and “FAN+” should be flipped

-J20: “GLV_GND” and “GLV_5V” should be flipped

PHYSICAL PLACEMENT ERRORS:

For the most part, all of the components on the PCB are in the adequate locations with the following exceptions:

-All 2N2222 Transistors used should be switched to the TO-92 package type. This is not a major error, simply a suggestion.

-2 8-pin terminal blocks were used for the Low voltage connections on the left side of the board. There should be a bit of spacing between J19 and J20 to allow the 2 8-pin terminal blocks to fit without having to be forced on. J20, J15, J11, and J16 should maintain their relative spacing to each other to accommodate the 0.1” pitch spacing of the terminal block. J17, J13, J12, and J19 should also maintain their relative spacing to each other.

-The hole diameters for U7, the SPST PCB 5V relay, should be made slightly larger as this component had to be forced onto the board

-The hole diameters for all terminal blocks (J1, J2, J3, J4, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J19, and J20) should also be made slightly larger as these components had to also be forced into position.

-The decals for all capacitors except the 220uF Electrolytic and the 22uF ceramic capacitor should be changed to be the standard 0805 package instead of what they are currently set as now.

TRACE/ELECTRICAL ERRORS:

For the most part, quality testing of the PCB found no major issues with the circuit design theory. However, the following issues were encountered and remedied in revision 1.

Base Transistor Sizing

-R9 decreased to 1.5Kohm

-R6 decreased to 1.5Kohm

-R2 and R10 decreased to 470 ohm

Missing Traces (Due to translation errors between DX Designer and PADS)

-Added trace between U5 Pin 11 to U14 Pin 4

-Added trace between J5 pin 2 and any Pack NEG connection

Circuit Design Errors

-The optoisolator for the Charge Detect signal (U14) causes an inadvertent logic inversion of the signal. Currently the signal is being inverted by tying the level shifted logic signal to all 4 inputs of the 2nd 4-input NOR gate (which makes the NOR gate act like an inverter) before sending to the 1st 4-input NOR gate which controls the safety relay. This modification should either be translated to the PCB board layout or other circuitry should be added to make the signal invert immediately after the optoisolator and before it is sent to the level shifter and DIO Pin 13. The software running on the Pack Manager accounts for this inversion (treats the signal as active low), so if an inverter is added before the signal is sent to the level shifter and DIO Pin 13, all software references to this signal should be inverted since it would now be active high.

-The P-FET (M1) that was supposed to be used for reverse polarity protection was not wired correctly in the PCB layout. The current fix removes the P-FET and simply uses a jumper wire to complete the path between what should have been the MOSFET drain and source inputs. This should be fixed or another reverse polarity protection circuit should be used to implement this feature.

-The LTC4151 chips used to measure current (U1 and U9) need to be wired differently in order to measure current correctly. According to the chip's datasheet the SENSE+ and VIN pins need

to be connected to get an accurate current reading. To remedy this, the SENSE+ and VIN pins should be tied to the Shunt_Pos (for discharging chip) or Shunt_Neg (for charging chip) net. ADR1 of the discharging chip should be tied to Pack_Neg and ADR0 of the discharging chip should be connected to the Shunt_Pos net. ADR1 and ADR0 of the charging chip should be tied to the Shunt_Neg net.

-Currently, the ADM2483 RS-232 to RS-485 Isolator chip is not working because the chip was fried. This will need to be replaced on the breakout board before the RS-485 protocol can be verified. It can also be replaced or removed if the 2015 team decides to use another method of communication with the central SCADA.

-The watchdog timer currently has a one second pulse output when it timeouts. It does not affect normal operation of the circuit, however it will reduce the lifetime of the Safety Loop PCB relay and causes an annoying clicking sound once a second when the watchdog is timing out. It is possible to either consider using an alternative watchdog timer without the pulsing, smooth out the pulsing signal using additional circuitry, or ignore the issue as it does not affect pack operation.

-In the current PCB layout, no circuitry was included to open the charging relays should the TS-8160-4200 computer sudden crash while the unit is charging. Ideally, if the watchdog timer times out for any reason, both the safety loop should be opened and the charging relays should be forced open as well. This will prevent the system from accidently overcharging cells should the computer stall and keep the DIO pin activating the charge relays high. Even though the software does not appear to be prone to failures during its observed operation period, THIS IS A MAJOR SAFETY CONCERN AND SHOULD BE ADDRESSED AS SOON AS POSSIBLE!