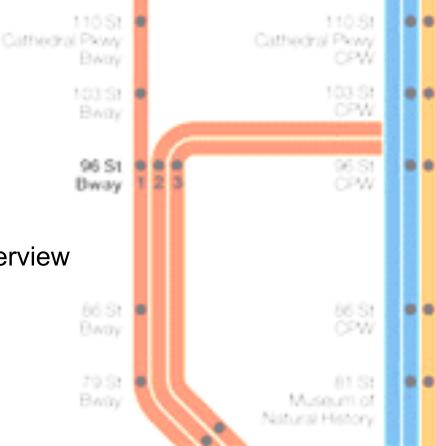
VSCADA Preliminary Design Report

PDR Covering the LFEV Software Design

Road Map

- Resource Availability
- Project Overview
- Risk Assessment
- Requirements Analysis
- System Design and Subsystem Overview Interface
- System Control States
- System Test Plan
- Software Maintainability Plan
- Cost Analysis
- Team Schedule Overview

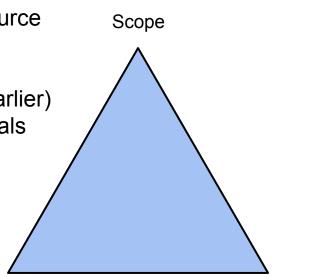




Resource Availability

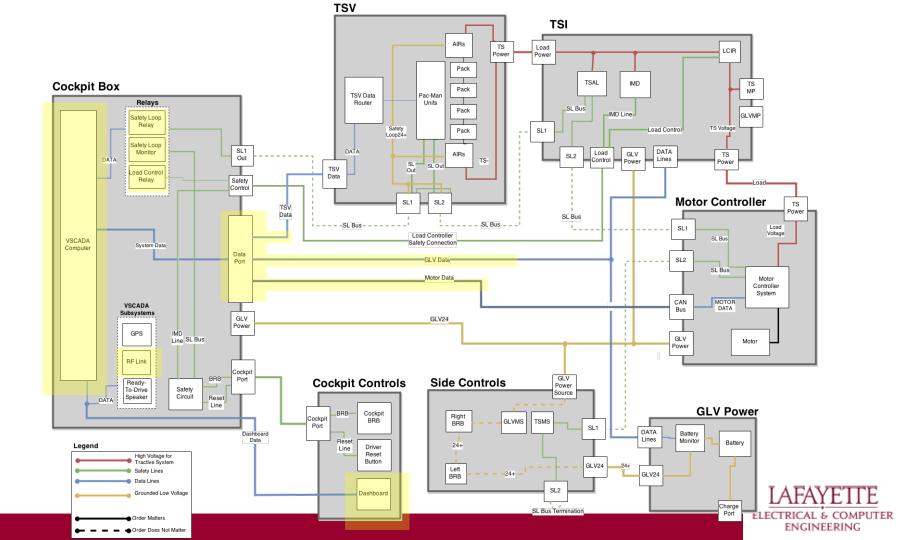
- Need to find a balance of the three resource components
- Time:
 - Limited time (need to be finished earlier)
 - Flexible schedule between individuals
- Resources
 - ∼\$1000
 - 24 hours available computer labs
 - Advice from Professors
 - Design from previous years
- Scope
 - Need to be cut down
 - Major structure done in week 9
 - Other requirements can be addressed later

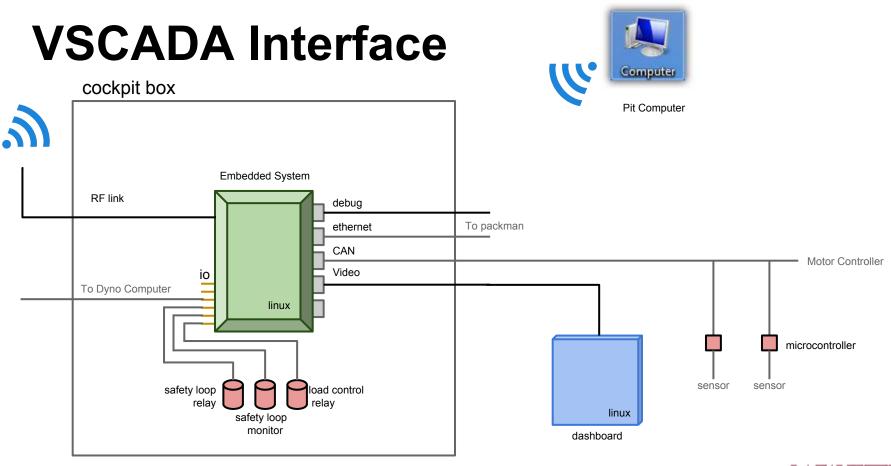
Time



Resources









Deliverable

- Maintenance Mode
 - Minimal restriction, ability to overwrite config files
- Drive Mode
 - Minimal display, load and clear
- Demonstration Mode
 - Pre-programed, labelled "Demo"
- API
- SDK
- Database
- Datalogging
- Configuration management, no recompile





Requirements Out of Scope

- Mobile App (~S009)
- Automatic Hardware Configuration (still check for sensors) (S017)
- GPS (S034)
- Long-term shutdown mode (S023)
- Plug-in and forget charging (S025)
- Plot data (S038)
- Dynamometer data acquisition (S042)
- Automated Charging of TSV (S013)
- Pre-Charge Discharge Circuits (EV 4.9)





Risk Assessment

- Coding Style
- Maintenance mode
- Warning/Fault Detection
- On-board Computer Handling
- Project Physical & Mental Health Effects





Requirements Analysis

- Back End Software
 - GLVIS Grounded Low Voltage Interface Software
 - TSVIS Tractive System Voltage Interface Software
 - MIS Motoro Interface Software
 - DB Data Base
 - DAA Data Acquisition and Analysis
- DOC Documentation
- Front End Software

UI-User Interface

Comm - Communication





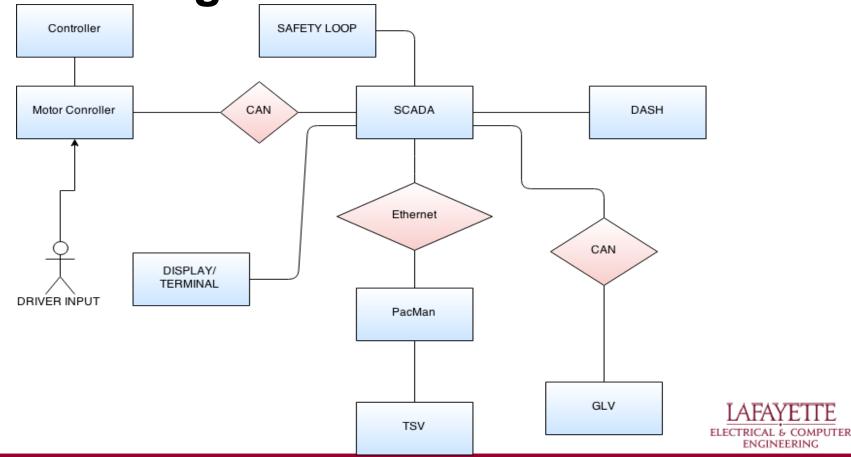
System Design

- VSCADA gathers information from other systems in electric vehicle and monitors these systems.
- Communicate with three different systems.
 - TSV(PacMan) using Ethernet
 - GLV using CAN bus protocol
 - Dyno(Motor Controller) using CAN bus protocol
- Safety loop is also included in case of emergency and system shut down.
- Operates on Linux OS.





System Design Overview



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System Hierarchical BreakDown

- VSCADA is divided into two subsystems frontend and backend.
- Backend and Frontend are further divided into smaller subsystems.

Frontend (User Interface)

- Dashboard Interface
- Mobile Interface
- Pit Station Interface
- Maintenance Mode
- Drive Mode
- Demo Mode

Backend

- Data Acquisition
- Vehicle control
- DataBase
- Computer System





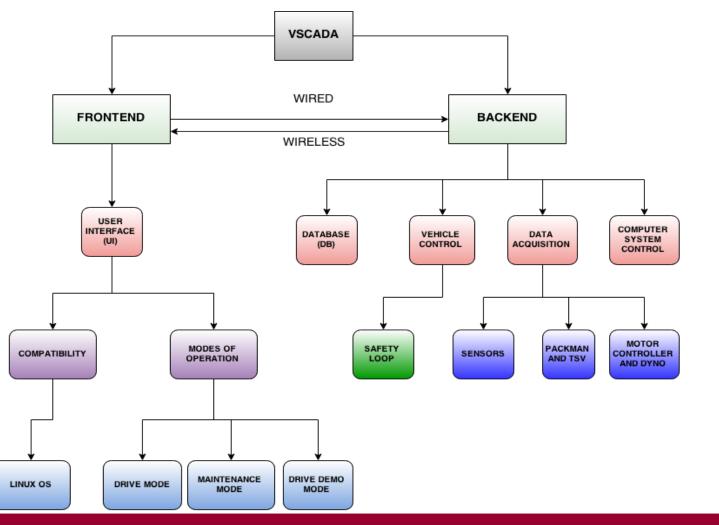


Fig. 2. System Hierarchical Breakdown



Interface

TSV

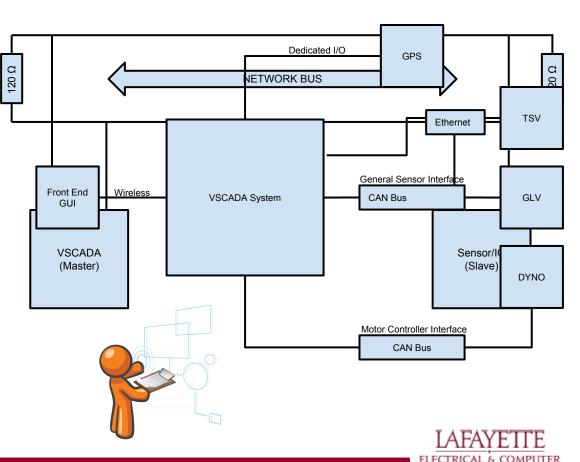
General Sensor Interface

GLV

General Sensor Interface

DYNO

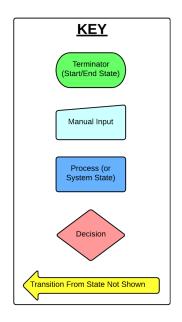
General Sensor Interface Motor Controller (CAN)



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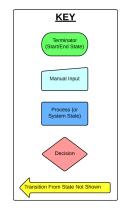
System Control States

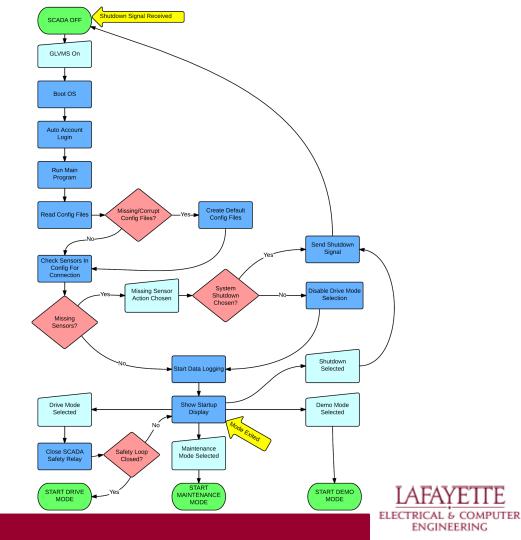
- Flowcharts created represent:
 - System Startup Logic
 - Drive Mode
 - Maintenance Mode
 - Demonstration Mode



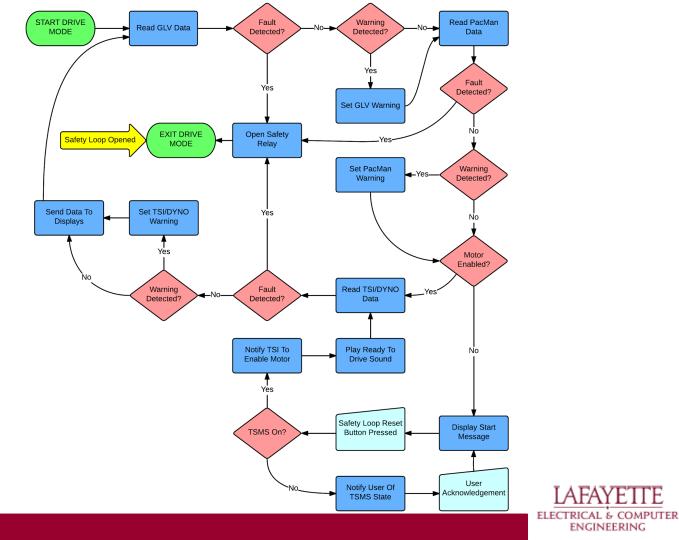


Startup States



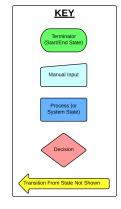


Drive Mode **States**

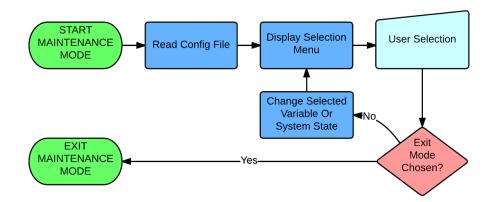


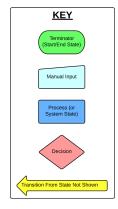
LAFAYETTE

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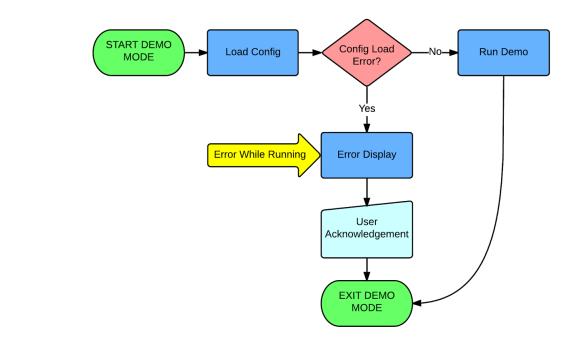
Maintenance Mode States



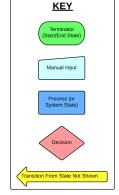




Demonstration Mode States







Acceptance Test Strategy

- Show that all requirements are met
- High-level outline to be expanded into ATP
- Compliance can be proved by
 - Analysis
 - Inspection
 - Test





ATP Test Outlines

An error has occurred. To continue: Press Enter to return to Windows, or Press CTRL+ALT+DEL to restart your computer. If you do this, you will lose any unsaved information in all open applications. Error: 0E : 016F : BFF9B3D4

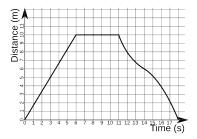
Windows

Press anu keu to continue

- T000 System Startup Test
 - Tests successful VSCADA startup on GLV power without human interaction
- T001 TSV Communication Test
 - Tests communication of VSCADA with Pacman using 2014 protocol
- T002 System Failure Recovery Test
 - Tests ability of system to recover in event of unexpected failure



ATP Test Outlines (cont.)



- T003 Motor Controller Test
 - Tests ability of VSCADA system communicating with motor controller
- T004 User Interface Test
 - Tests simultaneously functionality across all physical interfaces
- T005 Data Logging Test
 - Tests successful and accurate logging and plotting of measurands

ATP Test Outlines (cont.)

- T006 Wireless Link Communication Test
 - Tests successful communication between interfaces with minimal latency over wireless link
- T007 Hardware Detection Test
 - Tests autodetection of sensors without software recompilation
- T008 Rules Test
 - Tests setting of user defined alarm/shutdown rules



Cost Analysis

Embedded Computer

The 'Brain' of VSCADA

Embedded Linux System

LCD Display

Driver Dashboard Display

Miscellaneous Hardware

Supporting Hardware

- Connectors
- **Unexpected Costs**

Budget Summary

EXPENSE DESCRIPTION	TOTAL COST
Embedded Computer	\$200.00
Dashboard LCD Display	\$100.00
Wireless Radios	\$100.00
Power/Safety Loop Electronics	\$55.00
Interface Demonstration Microcontrollers	\$60.00
Miscellaneous Hardware Costs	\$235.00
TOTAL	\$750.00
	ELECTRICAL & COM ENGINEERING

Team Schedule Overview

- 15 week project
- first 9 weeks should design, build and test a simplified, working version
- Crucial deadlines:

milestones					
Name	Due Date				
PDR presentation	2/10/2015				
CDR presentation	3/11/2015				
phase one demonstration	3/25/2015				
acceptance test	4/13/2015				
final demonstration	5/1/2015				

Deliverables		13
PDR materials	2/8/2015	
user manual	2/13/2015	21
calibration and accuracy	2/16/2015	
acceptance test plan	2/19/2015	V
maintainability plan	2/26/2015	10
CDR materials	3/9/2015	<
QA audit report	4/8/2015	
acceptance test report	4/17/2015	
final report	4/27/2015	





Team Schedule Overview (cont.)

- Timeline
- Has 12 main tasks, each with sub tasks

			eb				Mar			Apr			May					
Jan 25	Feb 1	Feb 8	Feb 15	Feb 22	Mar 1	Mar 8	Mar 15	Mar 22	Ma	r 29	Apr 5	Apr 12	Apr 19	Apr 26	6 May 3	May 10	May 17	Μ
ା ପ୍	æ,																	
		PDR p	preparation															
		PDR	presentation	n														
			A	cceptance T	est Plan & C	Calibration a	nd Accuracy	1										
			Inter	ace control	document													
	-		User Manua	al														
				M	aintenance	Plan Final												
		-					reparation											
						CD	R presentat	ion										
								Software Im	pleme	entatio	n (1st phas	e)						
												Software Im	plementatio	n (2st pha	ise)			
														Class leve	I System Integ	ration		
								,				audit						
															Final Repor	t and Mainte	nance manu	al
													Acceptance	Test Rep	ort			
		_	Research T	opics														



Team Schedule Overview (cont.)

example part of the full task list	TASK NAME	ID	LENGTH (DAYS)	START	FINISH
	CDR Preparation	34			
shows tasks	Summary of Approved System Level Test Plan	35	2	2/20	2/23
completed	Safety Plan	36	1	2/13	2/13
for PDR	Updated System Design/System report draft	37	4	2/16	2/19
total of 103 tasks	Detailed Specifications for each subsystems	38	3	2/17	2/19
	Enhanced requirement analysis	39	3	2/17	2/19
	Program budget	40	2	2/23	2/24
	Revised Program schedule	41			
	Update with current progress	42	1	2/25	2/25
	List of completed/incomplete tasks	43	1	2/26	2/26
	CDR material check/revisit	44	3	3/3	3/5
	CDR write up/slide show	45	2	3/6	3/9
	CDR Presentation	46	1	3/11	3/11 I A FAVI

IAFAY ELECTRICAL & COMPUTER ENGINEERING

Team Schedule Overview (cont.)

- Individual tasks
 - Some are short tasks, required a day or two
 - Some are more complicated and may take more than one week, and the assignees are responsible for proposing his detailed weekly plan

task id 1	task name PDR preparation	Start Date	End Date
5	Requirements Analysis	1/29/2015	2/3/2015
7	Risk Assessment	2/3/2015	2/4/2015
101	Research sensors/protocols already on the system and possible additions	2/4/2015	2/9/2015
22	User manual: Block Diagram	2/9/2015	2/10/2015
26	User manual: FAQ	2/10/2015	2/12/2015
39	Enhanced requirement analysis	2/17/2015	2/19/2015
44	CDR material check/revisit	3/3/2015	3/5/2015
67	VCI: Dyno	2/27/2015	3/6/2015



Conclusion

- VSCADA is a subsystem of LFEV-Y3-2015 project. This preliminary design will serve as a baseline for the VSCADA team to enter a more detailed design phase.
- Moving forward, the VSCADA team will
 - expand and complete the Acceptance Test Plan
 - develop a user manual
 - finalize the breakdown of the system into implementable software modules
 - decide on the libraries and software tools to use
 - purchase the main interface, an embedded Linux device



Questions?



