LiFePO4 Battery Pack Per-Cell Management System

LAFAYETTE COLLEGE
ECE 492 – SENIOR DESIGN PROJECT

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Lafayette Photovoltaic Research and Development System (LPRDS)

- 2kW solar energy system that converts high voltage DC to 120V AC RMS signal of 60Hz
- Capstone project to introduce students to real engineering project issues and requirements
- Multi-year multi team senior Electrical and Computer Engineering design project
Design a system which will complete per-cell management requirement of the LPRDS statement of work

- Initially included full system integration into LPRDS tower, including 16, 4-cell packs and a master controller board

Diminished scope of project (due to time constraints) led to attempting only a subset of the requirements: one 4-cell pack of LiFePO4 cells

- Able to communicate to master device (PC or master board),
- Scalable to include multiple series packs
- Capability for full system integration
Why Balance?

- Extend useful lifetime
  - Or, not decrease the expected lifetime
- Increased health over lifetime
- Increased operational capacity
- Increase the accuracy of SOC calculations
Why Balance Our Way?

• Dictated by several factors:
  ○ Requirements
  ○ Physical limitations
  ○ Time constraints

• Design for simplicity:
  ○ Relatively simple implementation
  ○ Uses easy to gather information
  ○ Can be updated to reflect better cell characterization
Active Vs. Passive Balancing

- **Active**: Using capacitive or inductive loads to shuttle charge from higher charged cells to lower charged cells.
  - Is more efficient from a power perspective
  - Has scalability issues

- **Passive**: Bypasses cells (usually through a resistance) and burns off the excess charge from the cell.
  - Better large-stack scaling
  - Burn off can be significant
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Hardware Design
Hardware Design

- **Strict Physical Requirements**
  - Fit on top of a pack
  - Low enough to fit in rack
  - Interweave components between the cell terminals

- **Electrical Requirements**
  - High power path must handle up to 25 Amps
  - Minimize current drawn for circuitry
  - Electrical isolation for all communication signals
  - Bypass circuitry should bypass as much current as possible
Hardware Design - Bypass

- Main factors in bypass loop
  - Resistor
    - Value, package
  - Transistor
    - Switching parameters, package
  - Isolation
    - Solving the floating ground problem
  - Indication
    - Clear notification of when bypass occurs
Hardware Design - Bypass

Constant Power Curves For Varying Bypass Resistance

- No Airflow
- Airflow
- 3.3/R (Ohm's Law)
- 2.3/R (Ohm's Law)

Current (Amps) vs. Resistance (log(Ω))
Hardware Design – Temperature Analysis

- Temperature rise without heatsink ~ 4000 Kelvin
- Initial thermal requirement is 40°C above ambient: 65°C
- Temperature waiver raised requirement to 70°C above 30°C ambient = 100°C
Temperature Analysis

- Temperature rise heatsink ~ 400 K
- Empirically tested with IR gun, temperature rise does not exceed 53°C
- Temperature waiver requirement may still be necessary for individual component temperatures (i.e. bypass resistor, voltage regulator)
## Hardware Design - Sensors

- **Current, voltage, temperature monitoring**
  - Use these metrics during cell balancing

- **Redundant temperature monitoring is outside of the microcontroller**
  - Temperature failure notification not based in firmware

- **Buffers to boost signals and interface to low-impedance ADC’s**
Hardware Design - Microcontroller

- Controls the balancing algorithms as well as all communication going into or out of the board.

- Has three status LED’s to show activity and charge/discharge

- Programmable using ICSP, communicates with I2C
Hardware Design - Layout

- **Limited space**
  - Had to fit within the pack outline
  - Battery terminals were set
  - High current paths needed very wide traces

- **Heat dissipation**
  - Heatsink placement and attachment
  - Electrical insulation
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Software Design – Cell Balancing Algorithm

• Utilizes direction of current through current sensor to determine charging or discharging state
• In charging state, bypass based on monitoring of 50 mV differences in cell voltages
• Maximum and minimum charge decided by variable voltage thresholds determined by register in PIC
• Monitors temperature to protect against overheating
Software Design – State of Charge Algorithm

• Based on Coulomb Counting

• Uses data from the current sensor to sum the current over time

• Sum and sample period are output through I2C, and the user can calculate SOC by

\[
\text{SOC} (\%) = \frac{\text{Sum} \times \text{sample period}}{\text{Capacity (A} \times \text{Hr)}} \times 100
\]
OBPPs respond only to board address matched by value in program memory.

Memory address is mapped to a function in firmware.

I2C can read all defined memory addresses.

Certain variables can be changed to alter operation of OBPP.

I2C can be used to manually set bypass.

Can address up to 168 packs in system.
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Simulation – SOC Curves

- SOCs begin at largely different values
- Over about 16 charge/discharge cycles, SOCs converge to within 5% of each other
- Standard deviation of SOCs of the cells begins at 12% and decreases to about 2% SOC
Simulation – Standard Deviation and Power

- Bypass curves coincide with sloped regions of standard deviation curve
- As pack converges, less bypass is needed
- Standard deviation decreases and levels off over multiple charge/discharge cycles, demonstrating convergence
Standard Deviation in %SOC and Joules

Standard Deviation in %SOC
(12% - 2%)

Standard Deviation in Joules
(3.4 \times 10^6 J - 0.5 \times 10^6 J)
Simulated Merit of Efficiency

For grouping of cells with initial SOCs: 90%, 25%, 12%, 10%

\[
\frac{\max(\sigma) - \min(\sigma)}{\max(J) - \min(J)} = \eta(J/J)
\]

\[
\frac{3.35 \times 10^6 - 1.49 \times 10^5}{1.38 \times 10^5} \approx 23.1
\]
Merit of Efficiency

- Using capacitive or inductive balancing may be more efficient than resistive bypassing

- We have a way of determining and justifying the efficiency of our system.

  \[
  \text{Imbalance / Cost} = \text{Efficiency (J/J)}
  \]

- Why does it work?

  Multiple Cycle, Partial Resistive Bypassing
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Acceptance Testing

- Comprehensive testing to prove requirements have been met
- Composed of two main tests and one secondary test
- 24 hour operation test
- Test 1: Cell balancing, hardware requirements, indicators and communication
- Test 2: Comprehensive I2C verification
- Test 3: Addressing basic/complex problems using the User’s Manual
Acceptance Testing Setup
Acceptance Testing - Test 1

- Pack is deliberately unbalanced
- Test setup fully charges and discharges the system multiple times
- Data is taken from all cells continuously
- Simulink is used to automate the change from charging to discharging
- After five cycles, a script polls the I2C line for another 16 hours
Acceptance Testing – Test 1

Cell Voltage vs. Time - ATP T001

- 100% SOC
- 95% SOC
- 80% SOC
- 70% SOC
Empirical Results

- It works!
  - Based on a metric that we created
    - For the express purpose of passing this test

- Approximate beginning standard deviation = 12%

- Approximate ending standard deviation = 9%

- More charge/discharge cycles needed for better graphs and more rigorous verification
Acceptance Testing - Test 2

- Comprehensively test I2C
- Make sure every voltage, temperature, current, and other relevant measurements are accurate and concur with digital multimeters and thermometers
- Also, make sure manual mode works as desired and bypass can be initiated for the desired amount of time.
- Lastly, make sure the I2C system remains responsive throughout the duration of the test.
Empirical Results

- Passed all parts of Acceptance Test 2 except 2\textsuperscript{nd} part of temperature verification
  - Initial hypothesis for reason of failure is ineffective testing method procedure
    - Heat dissipated through heatsink before accurate temperature from thermometer could be read
    - IR gun does not accurately report temperature of reflective surfaces
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Requirements Met

- **R002 – Energy Storage**
  - LPRDS-CMS-2011 permits per-cell battery management
  - System charges to maximum recommended capacity (over several charge/discharge cycles)
  - System bypasses cells which become full first to balance cells
  - System monitors cell voltage to avoid over-discharge
    - Indication LEDs and DONE signal
  - I2C system can monitor voltage and current of every cell in pack and the SOC of each pack
  - Standalone operation of CMS pack
- **GPR002 – Environmental**
  - System is reliable under normal functional operation in ambient lab temperatures of 70°C over ambient of 30°C

- **GPR003 – EMI/EMC**
  - Does not emit any unintentional electromagnetic radiation

- **GPR004 – Hazmats**
  - There are no hazardous materials used in this design

- **GPR006 – Reliability**
  - The system wide MTBF is greater than 1000 hours over system lifetime
  - 24 hour test demonstrated firmware reliability (also demonstrated hardware failure, not design flaw)

- **GPR007 – Maintainability**
  - System wide MTTR is less than 1 week over system lifetime
  - Repairs during ATP took less than 1 week to complete

- **GPR008 – Manufacturability**
  - All components and subassemblies have sustainable source of supply over system lifetime
Requirements Missed

- Accurately read temperature during T002
- Continuous Fuel Gauge indicator (trinary)
- Schedules (every single one)
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Conclusions

- Standard deviation of cell voltages is a fair metric of the effectiveness of the CBA

- Effective operational capacity of the balanced cells demonstrates a noticeable increase over the unbalanced cells

- Capacity variation between cells has a significant impact on the predictability of the algorithm
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Budget – Full Project Spending

Total expenditures: ~$1,373
Budget – Pack Cost

Total cost: ~$141
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Future Work

- Modification of the CBA to accommodate certain conditions
  - All cells bypassed
  - Cells nearing convergence
  - Sliding bypass window

- Full stack integration incorporating a master device

- Full system integration with the LPRDS system
Questions?