LPRDS-BMS 2010

Lafayette Photovoltaic Research and Development System: Battery Management System

ECE 492 – 2010

Acceptance Test Plan
DRAFT

Last Revision 04/27/10 by Laura Pritchard
1.0 SUMMARY

The Acceptance Test Plan describes how we plan to prove that the LPRDS-BMS complies with all requirements and specifications. We will test the integrated system to verify that it manages battery charging, produces the required AC voltage, accurately records measurements, and properly responds to faults as specified in our requirements document. In addition to demonstrating proper operation of the system, we will inspect the project website to verify that our other deliverables have been completed, and inspect the project work areas to verify that procedures pertaining to the disposal of project materials have been followed.

Figure 1: LPRDS Block Diagram
2.0 Compatibility Matrix

These tables list each requirement by number and description. The **MET** column contains a letter representing how the requirement was met and a number representing the section of the Acceptance Test Report where the requirement is addressed.

T – Test
A – Analysis/Simulation
I – Inspection
N – No Test Necessary
QAR – See the subsystem Quality Assessment Report
X – Requirement Not Met

2.1 Technical Requirements

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>MET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>R001:</strong> Raw Power Interface (RPI)</td>
<td></td>
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<tr>
<td>R001-01</td>
<td>Any connection to high voltage DC from the PV array must be through the RPI.</td>
<td>RPI QAR</td>
</tr>
<tr>
<td>R001-02</td>
<td>The RPI contains main logic for safety interface; all other LPRDS subsystems must be compliant with this safety interface.</td>
<td>N</td>
</tr>
<tr>
<td>R001-03</td>
<td>The system requires low voltage to operate; this must be provided by the LPRDS per R010.</td>
<td>RPI QAR</td>
</tr>
<tr>
<td>R001-04</td>
<td>Through an RS-485 connection, the RPI will enable SCADA to monitor voltage and current on all interfaces, internal temperature in critical points, and operational or fault state.</td>
<td>RPI QAR</td>
</tr>
<tr>
<td><strong>R002:</strong> Energy Storage System (ESS)</td>
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<tr>
<td>R002-01</td>
<td>LPRDS-BMS-2010 shall re-use the existing LiFePO4 cells incorporated in the existing system and to every extent possible re-use the existing ESS.</td>
<td>N</td>
</tr>
<tr>
<td>R002-02</td>
<td>To the extent they do not conflict and are not superseded, old ESS requirements will apply to the new ESS specifications per R002B.</td>
<td>N</td>
</tr>
<tr>
<td>R002-03</td>
<td>ESS provides low-voltage DC power for itself and other LPRDS systems; this design choice shall be re-evaluated in light of the “maintenance power mode” required by R010.</td>
<td>ESS QAR</td>
</tr>
<tr>
<td>R002-04</td>
<td>The ESS shall be capable of standalone operation. It shall be possible to properly charge and discharge the ESS without needing an outside computer system for control or monitoring.</td>
<td>X, ESS QAR</td>
</tr>
<tr>
<td>R002-05</td>
<td>Controls shall be provided, if needed, to permit standalone management.</td>
<td>X, ESS QAR</td>
</tr>
<tr>
<td>R002-06</td>
<td>Indicators shall be provided that display operational state (charge/discharge) and charge state (fuel gauge).</td>
<td>X, ESS QAR</td>
</tr>
<tr>
<td>R002-07</td>
<td>A remote SCADA system shall be able to monitor the voltage, current, and state of charge of the aggregate ESS battery and every individual cell, and overall ESS parameters.</td>
<td>ESS QAR</td>
</tr>
<tr>
<td>R002-08</td>
<td>Low-level data interface to SCADA shall be RS-485, but it is not necessary to retain the EDS data formats or communication protocols established in ETS-2009.</td>
<td>N</td>
</tr>
<tr>
<td>R002-09</td>
<td>The LPRDS-BMS-2010 shall re-engineer the ESS to permit per-cell battery management.</td>
<td>ESS QAR</td>
</tr>
<tr>
<td>R002-10</td>
<td>The new system shall charge every cell in the ESS to its maximum</td>
<td>X</td>
</tr>
<tr>
<td>R002-11</td>
<td>A means shall be provided to bypass the cells that become full first, allowing complete charge to be delivered to cells that charge more slowly.</td>
<td>ESS QAR</td>
</tr>
<tr>
<td>---</td>
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</tr>
<tr>
<td>R002-12</td>
<td>On discharge, every cell shall be monitored and over-charge of any individual cell must be avoided.</td>
<td>ESS QAR</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R002B:</th>
<th>Legacy ESS Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>R002B-01</td>
<td>ESS shall be connected to the safety interface and designed so that a fault in the system will cause the ESS to disconnect HV from outside terminals and go into a fault state. Should the ESS detect a fault, it will break the safety interface.</td>
</tr>
<tr>
<td>R002B-02</td>
<td>A fault indicator light shall be provided on the ESS that illuminates when a fault has caused the shutdown of the ESS.</td>
</tr>
<tr>
<td>R002B-03</td>
<td>ESS must be built with a normally open isolation relay or equivalent wiring so that when the safety interface is interrupted or absent, no high voltages will be delivered.</td>
</tr>
<tr>
<td>R002B-04</td>
<td>ESS shall be internally protected from excessive charge or discharge rates, excessive overcharge, and excessive discharge.</td>
</tr>
<tr>
<td>R002B-05</td>
<td>A shutdown switch, compliant with NEC and the safety plan, must be provided as part of the ESS. When the switch is open, DC energy from the ESS shall not be conducted to the LPRDS-BMS. This switch must be easy to operate, mounted on the ESS in a visible location, and have the ability to be key-locked in the disabled state.</td>
</tr>
<tr>
<td>R002B-06</td>
<td>An indicator light shall be provided on the ESS that illuminates when the ESS is connected and HV DC is present.</td>
</tr>
<tr>
<td>R002B-07</td>
<td>Energy storage in the ESS must be in closed containers with safety interface, indicators, and controls as required herein.</td>
</tr>
<tr>
<td>R002B-08</td>
<td>Containers must include an appropriately rated fuse or circuit breaker.</td>
</tr>
<tr>
<td>R002B-09</td>
<td>Safety relays must be rated to interrupt the rated fuse current at the maximum expected voltage.</td>
</tr>
<tr>
<td>R002B-10</td>
<td>Containers must have closable access ports allowing a probe to make contact with each extreme of the HV system (to permit testing the isolation stipulated by the safety plan).</td>
</tr>
<tr>
<td>R002B-11</td>
<td>Containers must have an indicator, such as an LED, that will illuminate whenever the container contains a voltage greater than 30V, visible in bright room light.</td>
</tr>
<tr>
<td>R002B-12</td>
<td>Multiple energy storage containers connected in series may be isolated by a total of two relays.</td>
</tr>
<tr>
<td>R002B-13</td>
<td>Interconnects between the containers are protected by non-conductive conduit anchored solidly to the containers.</td>
</tr>
<tr>
<td>R002B-14</td>
<td>Voltages outside the energy storage container must decay to below 30V within ten seconds if the relays are disconnected (filter caps or bleeder resistors across them).</td>
</tr>
<tr>
<td>R002B-15</td>
<td>Discharge power capacity of the ESS shall be able to meet the power requirements of the EDS when that system is delivering the maximum required power to the load.</td>
</tr>
<tr>
<td>R002B-16</td>
<td>SCADA shall be able to monitor voltage and current on all interfaces, internal temperature at critical points, and operational or fault state. In the case of sinusoidal AC interfaces, measurement of the phase angle between voltage and current is also required.</td>
</tr>
</tbody>
</table>
### R003A: Energy Delivery System (EDS) Requirements Met in Switch Controller (SC)

| R003A-01 | EDS shall be properly designed with consideration of the high voltages and currents per the electrical safety plan. | SC QAR |
| R003A-02 | Once activated, with no faults present, first priority of EDS is to convert DC energy from the PV array to meet AC power delivery needs. | T 5.1.1 |
| R003A-03 | The EDS shall be able to switch between sources of power (PV array or ESS) without interrupting the delivery of power to the load. | T 5.1.1 |
| R003A-04 | If power delivery can be fully met by converting energy from the PV array, any excess energy available shall be used to charge the ESS until the ESS is charged to capacity. | T 5.1.1 |
| R003A-05 | If sufficient power cannot be derived from the PV array to meet AC power delivery needs, the EDS will supplement PV power with stored energy from the ESS. | T 5.1.1 |
| R003A-06 | If insufficient power is available from both the PV array and the ESS to maintain load regulation, the EDS shall drop the load and enter an undersupply fault state. | T 5.1.1 |
| R003A-07 | EDS shall not over-charge or over-discharge the ESS, nor shall the EDS charge or discharge the ESS at rates beyond its rated capacity. | T 5.1.1 |
| R003A-09 | An RS-485 interface to the SCADA system shall be provided with format as required for supervisory functions. | N |
| R003A-09 | SCADA shall be able to monitor voltage and current on all interfaces, internal temperature at critical points, and operational or fault state. In the case of sinusoidal AC interfaces, **measurement of the phase angle** between voltage and current is also required. | X SC QAR |

### R003B: Energy Delivery System (EDS) Requirements Met in Filter-Inverter Box (FIB)

| R003B-01 | The EDS will be connected to the safety interface connecting the RPI and ESS. Breaking the safety interface shall cause all systems to disconnect HV from outside terminals and enter a fault state. Should the EDS detect a fault, it will break the safety interface. | FIB QAR |
| R003B-02 | The EDS shall remain in shutdown until all faults are cleared and the main startup switch is actuated. | FIB QAR |
| R003B-03 | The EDS shall be able to deliver high quality, regulated, 120V RMS, sinusoidal 60Hz AC electricity, continuously, at a maximum sustained current of 10A RMS, to a load of any power factor. | FIB QAR |
| R003B-04 | 60Hz sinusoidal frequency shall be accurate to within 0.05%; locking to commercial mains frequency is desirable but not required as long as frequency tolerance is maintained. | FIB QAR |
| R003B-05 | Transient response overshoot shall be less than 5%, for any step load change within the sustained capacity of the system. | FIB QAR |
| R003B-06 | Step response settling time within 2% shall be less than 33ms. | FIB QAR |
| R003B-07 | Load regulation steady state error shall be better than 3%. | FIB QAR |
| R003B-08 | Total harmonic distortion into linear load shall be less than 3%. | FIB QAR |
| R003B-09 | An RS-485 interface to the SCADA system shall be provided with format as required for supervisory functions. | N |
| R003B-10 | SCADA shall be able to monitor voltage and current on all interfaces, internal temperature at critical points, and operational or fault state. In the case of sinusoidal AC interfaces, **measurement of the phase angle** between voltage and current is also required. | X FIB QAR |
and current is also required.

<table>
<thead>
<tr>
<th>R004:</th>
<th>Supervisory Control and Data Acquisition (SCADA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R004-01</td>
<td>SCADA shall serve as the Maintenance User Interface for the LPRDS.</td>
</tr>
<tr>
<td>R004-02</td>
<td>SCADA will include display, control, or interface hardware (some existing (DFE), &quot;PicoLCD&quot; display, alarm buzzer, alarm silence button, and shutdown switch).</td>
</tr>
<tr>
<td>R004-03</td>
<td>If the 2010 team discards a required 2009 component, they must provide new replacement or alternative that meets all requirements.</td>
</tr>
<tr>
<td>R004-04</td>
<td>SCADA interface shall be expandable to control and monitor additional subsystems without the need for additional SCADA hardware.</td>
</tr>
<tr>
<td>R004-05</td>
<td>Software must run on the existing FIT PC hardware platform included (DFE) in the system.</td>
</tr>
<tr>
<td>R004-06</td>
<td>The operating system shall be Ubuntu Linux currently installed.</td>
</tr>
<tr>
<td>R004-07</td>
<td>SCADA software must start automatically when the FIT PC is started, reaching operational state without human interaction.</td>
</tr>
<tr>
<td>R004-08</td>
<td>Performing an orderly shutdown of the FIT PC (e.g. Unix &quot;halt&quot; command) shall automatically shutdown the SCADA software properly without causing corruption.</td>
</tr>
<tr>
<td>R004-09</td>
<td>Backup system or recovery strategy must be developed to allow the SCADA system to be repaired after hardware failure in less time than the MTTR given in GPR007.</td>
</tr>
<tr>
<td>R004-10</td>
<td>All SCADA software should automatically initialize when SCADA computer is powered up, it should not be necessary to run programs to start system after reboot or power outage.</td>
</tr>
<tr>
<td>R004-11</td>
<td>Delivered SCADA software shall be fully documented with source code, design, and end-user documentation allowing a trained human technician to easily control and monitor the LPRDS.</td>
</tr>
<tr>
<td>R004-12</td>
<td>SCADA application software must be written in conformance with a documented API (R006) using a delivered SDK.</td>
</tr>
<tr>
<td>R004-13</td>
<td>RS-485 interface shall be connected to all major subsystems and shall provide a mechanism by which each can be controlled and monitored by the central SCADA system.</td>
</tr>
<tr>
<td>R004-14</td>
<td>Monitor voltage, current, and power delivered to the load.</td>
</tr>
<tr>
<td>R004-15</td>
<td>Monitor AC power factor at the load.</td>
</tr>
<tr>
<td>R004-16</td>
<td>Monitor voltage, current, and power supplied by the PV array.</td>
</tr>
<tr>
<td>R004-17</td>
<td>Monitor rate of charge or discharge of the aggregate ESS and individual cells and estimate of their state of charge.</td>
</tr>
<tr>
<td>R004-18</td>
<td>Monitor temperatures of all subsystems.</td>
</tr>
<tr>
<td>R004-19</td>
<td>Hardware and software shall be provided to access, record, and display data from the &quot;Sunny Boy&quot; inverter in a form that is integrated with the overall LPRDS data display.</td>
</tr>
<tr>
<td>R004-20</td>
<td>It shall be possible to measure individual parameters up to 60 times a minute.</td>
</tr>
<tr>
<td>R004-21</td>
<td>All parameters shall have their values logged electronically along with a time stamp at least once a minute.</td>
</tr>
<tr>
<td>R004-22</td>
<td>Plots covering the last hour, day, week, month, and year shall be generated.</td>
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<tr>
<td>R004-23</td>
<td>SCADA data storage shall have sufficient capacity for retaining data records over the lifetime of the system.</td>
</tr>
<tr>
<td>R004-24</td>
<td>Data storage shall be accumulated in a portable, non-proprietary format readily usable by commonly available data and analysis tools.</td>
</tr>
<tr>
<td>R004-25</td>
<td>All SCADA functions shall be fully available to remote PCs through the Lafayette College computer network via a single IP address associated with the hostname (lprds.aec.lafayette.edu).</td>
</tr>
<tr>
<td>R004-26</td>
<td>Security features shall be provided that will limit access to authorized users, only ports 80, 443 (http, https) and 22 (ssh) are allowed for communication.</td>
</tr>
<tr>
<td>R004-27</td>
<td>SCADA shall allow human interactive control of the system startup.</td>
</tr>
<tr>
<td>R004-28</td>
<td>SCADA shall allow human interactive control of the system shutdown.</td>
</tr>
<tr>
<td>R004-29</td>
<td>SCADA shall allow human interactive control of the force disconnect of load.</td>
</tr>
<tr>
<td>R004-30</td>
<td>SCADA shall allow human interactive control of the force disconnect of PV power (run entirely on batteries).</td>
</tr>
<tr>
<td>R004-31</td>
<td>SCADA shall allow human interactive control of the force disconnect of ESS (run the system entirely on PV).</td>
</tr>
<tr>
<td>R004-32</td>
<td>SCADA shall allow human interactive control to simulate fault.</td>
</tr>
<tr>
<td>R004-33</td>
<td>SCADA shall allow human interactive control to clear fault.</td>
</tr>
<tr>
<td>R004-34</td>
<td>SCADA shall allow human interactive control of the Sunny Boy functions.</td>
</tr>
<tr>
<td>R004-35</td>
<td>SCADA shall automatically log any events, exceptions, faults, or changes in operational state of the LPRDS, including safety interface events.</td>
</tr>
<tr>
<td>R004-36</td>
<td>At a minimum, it shall be possible to have the SCADA system automatically log an event, enable an alarm, or declare a fault to shutdown the LPRDS-BMS.</td>
</tr>
<tr>
<td>R004-37</td>
<td>When a fault occurs, SCADA should sound the loud (audible from the ECE Dept. Sect. office) aural alarm provided. A &quot;silence alarm&quot; button shall be provided with an indicator.</td>
</tr>
<tr>
<td>R004-38</td>
<td>Pressing the silence button shall quiet the alarm till the next fault occurs.</td>
</tr>
</tbody>
</table>

**R006: Application Programming Interface and System Development Kit**

| R006-01 | The LPRDS-BMS-2010 shall provide a documented API and SDK that a programmer can use to write applications to control and monitor all interfaces and functions supported by SCADA. | SCADA QAR |
| R006-02 | The scope of API must be sufficient to support both low-level debugging applications and high-level automated applications. | SCADA QAR |
| R006-03 | The SDK must include a complete tool chain, with compilers, linkers, libraries, include files, utilities, compilers, as well as developer level documentation. | SCADA QAR |
| R006-04 | The complete SDK, including API documentation and application source under configuration, shall be delivered to or linked to the project web site. | SCADA QAR |

**R008: Demonstration Application**

| R008-01 | The LPRDS-BMS-2010 shall provide a fully documented, user friendly Demonstration Application. | SCADA QAR |
| R008-02 | The application must allow a non-technical, minimally trained human user to successfully witness an automatic demonstration of the capabilities of the system and DFE system per GPR011. | SCADA QAR |
| R008-03 | The application must include a large display that is visible through the window of room AEC401 allowing passers-by to witness some aspects of the demo. | SCADA QAR |
| R008-04 | The Demo App should be designed to provide an interesting demo with interactive options and a robust tolerance for possible mistakes made by operator. | SCADA QAR |
| R008-05 | App software must be written in conformance with LPRDS-BMS-2010 API (R006), built with tools provided in the SDK, and run on hardware included and powered by the LPRDS-BMS-2010. | SCADA QAR |

**R009: Modifications of the LPRDS**

| R009-01 | Modifying the HV and PV portions of the LPRDS, or modifying the RPI, or physical alteration of the building is not permitted except with permission of the ECE Department. | N |
| R009-02 | The mechanical packaging and cabling existing for the ESS and overall LPRDS rack (including safety switches, displays, and alarms) shall be reused as much as possible. | N |
| R009-03 | Mechanical attachments for enclosures, conduits, and other equipment may be added to the LPRDS or Room 401 with prior approval of the ECE Department. | N |

**R010: Power Input Independence**

| R010-01 | The installed LPRDS-BMS-2010, including the RPI, SCADA, and the Demo App, shall be able to operate without any power derived from building mains without unduly draining the ESS when sunlight is not available. | X 4.2.1 |
| R010-02 | A maintenance power mode shall be provided, in which the system shall be fully functional with power derived entirely from building mains. | A 4.2.1 |
| R010-03 | All voltages needed shall be generated by LPRDS-BMS-2010 circuitry per GPR005. | ESS QAR |

**R011: Safety Interface**

| R011-01 | The existing RPI safety interface shall be fully retained. | RPI QAR |
| R011-02 | The interface shall be connected to all major subsystems and provide a mechanism by which entire system can be quickly and reliably shutdown should a fault be detected. Should it be broken at any location shutdown will immediately occur. | T 5.1.3 |
| R011-03 | The safety interface must be completely independent of any other interface. | RPI QAR |
## 2.2 General Project Requirements

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPR001:</td>
<td><strong>Documentation</strong></td>
<td></td>
</tr>
<tr>
<td>GPR001-01</td>
<td>Complete and accurate documentation must be provided with all projects including mechanical and electrical fabrication, test results, software development kits, maintenance manual, user manual, and specification compliance matrices, and technical papers.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-02</td>
<td>All documentation shall be accumulated in electronic form, centralized in a project web site, and thoroughly indexed. Original paper documents should be disposed of as per GPR012.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-03</td>
<td>Text documents shall be written in a professional style commensurate with quality standards established by Lafayette College ECE writing courses (ES225 and ECE211).</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-04</td>
<td>All documentation must be used so that no proprietary applications are necessary.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-05</td>
<td>Test reports for hardware and software must show date/time of testing, name and signature of the tester, and name/signature of any witnesses.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-06</td>
<td>All electronic PCB designs must include the following documents: dated and numbered schematics or mechanical drawings on Lafayette College Drawing format, circuit net-lists, bills of materials, artwork, assembly drawings, and all other files.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-07</td>
<td>Documentation must be provided both for original designs and for any subcontracted designs. For purchased vendor components within the design, all vendor manuals and documentation shall be maintained.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-08</td>
<td>For software and firmware designs: source code, executable binaries for all applications, Verilog, constraints and configuration bitstreams for FPGAs, and ROM image files in commonly accepted JED or HEX formats for all PLDs.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR001-09</td>
<td>Technical maintenance manual including any information about advanced calibration techniques that could be applied by the expert maintainer.</td>
<td>1 5.2.1</td>
</tr>
<tr>
<td>GPR002:</td>
<td><strong>Environment</strong></td>
<td></td>
</tr>
<tr>
<td>GPR002-01</td>
<td>All projects must demonstrate reliable and normal functional operation in ambient lab temperatures of 15°C to 30°C, 10% to 80% RH, non-condensing.</td>
<td>A 6.2.5</td>
</tr>
<tr>
<td>GPR002-02</td>
<td>The overall system must tolerate a storage environment of 0°C to +60°C, 5% to 95% RH, non-condensing.</td>
<td>A 6.2.5</td>
</tr>
<tr>
<td>GPR002-03</td>
<td>Designs should use electronic components rated for commercial temperature range (0-70°C) or better.</td>
<td>A 6.2.5</td>
</tr>
<tr>
<td>GPR003:</td>
<td><strong>Electromagnetic Interference and Compatibility</strong></td>
<td></td>
</tr>
<tr>
<td>GPR003-01</td>
<td>Unintentional electromagnetic radiation radiated or conducted from designs must meet US CFR Title 47 Part 15 subpart B regulations for Class A digital equipment.</td>
<td>T (FIB)</td>
</tr>
<tr>
<td>GPR003-02</td>
<td>Intentional radiators must meet subpart C regulations, exemptions from 15.103 are not allowed.</td>
<td>N</td>
</tr>
<tr>
<td>GPR004:</td>
<td><strong>Hazardous Materials</strong></td>
<td></td>
</tr>
<tr>
<td>GPR004-01</td>
<td>If use of a hazardous material is essential to the function of the design and there is no non-hazardous alternative, the use of the hazardous material must comply with the Lafayette College Chemical Hygiene Plan</td>
<td>I 6.2.5</td>
</tr>
<tr>
<td>GPR004-02</td>
<td>All materials used in electronic circuit fabrication must meet 2002/95/EC</td>
<td>I 6.2.5</td>
</tr>
</tbody>
</table>
RoHS directives. NiCd or Lead-Acid batteries may not be used in new designs.

<table>
<thead>
<tr>
<th>GPR004-03</th>
<th>Any portion of the design or prototype that is discarded must be discarded according to the Lafayette College Chemical Hygiene Plan. Projects should discard electronic waste in an ecological-friendly manner as per the 2002/96/EC WEEE directive.</th>
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</table>

### GPR005: Safety and Good Practice

<table>
<thead>
<tr>
<th>GPR005-01</th>
<th>Color-coded wiring in accordance with applicable industry standard color codes (e.g. NFPA 79 or UL508 for power wiring, EIA/TIA 568 for network wiring, etc.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPR005-02</td>
<td>Clear labeling of all controls and indicators</td>
</tr>
<tr>
<td>GPR005-03</td>
<td>An obvious and clearly labeled system-wide power shutdown switch</td>
</tr>
<tr>
<td>GPR005-04</td>
<td>Silkscreen on PCBs that include reference designators, noted power supply voltages and other critical signals. Silkscreen must show a Lafayette College logo, the words &quot;Made in USA,&quot; an RoHS logo, an assembly number, a revision number, and a serial number</td>
</tr>
<tr>
<td>GPR005-05</td>
<td>Fuses shall be socketed; breakers shall be resettable. All are readily accessible per maintainability requirements.</td>
</tr>
<tr>
<td>GPR005-06</td>
<td>Service loops on all cable harnesses</td>
</tr>
<tr>
<td>GPR005-07</td>
<td>Access panels on enclosures</td>
</tr>
<tr>
<td>GPR005-08</td>
<td>Embedded computer processors shall have reset buttons. These buttons must be readily acceptable for maintenance, but not so easy to hit that they degrade reliability.</td>
</tr>
<tr>
<td>GPR005-09</td>
<td>Power dissipation rating of parts shall be 50% overrated over the required temperature range.</td>
</tr>
<tr>
<td>GPR005-10</td>
<td>Current drain analysis must be provided for all power supplies. Each supply voltage must have a current rating with 50% safety factor over the anticipated peak current.</td>
</tr>
<tr>
<td>GPR005-11</td>
<td>Working voltage of capacitors shall be 25% overrated above the peak voltage anticipated, including all expected glitches, spikes, and tolerance limit.</td>
</tr>
<tr>
<td>GPR005-12</td>
<td>All resistors or other parts dissipating more than 25mW shall be identified and analysis shall be provided that shows all such parts are properly rated for peak and average power dissipation and have a proper heat sink and fan.</td>
</tr>
<tr>
<td>GPR005-13</td>
<td>Components must be cooled such that the surface temperature is no greater than 40 degrees C above ambient temperature.</td>
</tr>
<tr>
<td>GPR005-14</td>
<td>Fans should be protected with grilles and filters. EMI analysis must consider the fan opening and specify EMI-tight grillwork if necessary.</td>
</tr>
<tr>
<td>GPR005-15</td>
<td>Any project that develops AC RMS or DC potential differences greater than 30V between any two points within the design must develop and implement an electrical safety plan before any circuits are powered.</td>
</tr>
<tr>
<td>GPR005-16</td>
<td>Project activities must adhere to the general Lafayette College safety policy, possibly augmented by any ECE Department or ECE Laboratory safety rules.</td>
</tr>
<tr>
<td>GPR005-17</td>
<td>ECE Director of Laboratories must approve the electrical safety plan and a team member must be appointed project safety officer.</td>
</tr>
<tr>
<td>GPR005-18</td>
<td>All equipment developed must comply with The National Electrical Safety Code (NESC) - ANSI C-2. Installations of electric conductors and equipment that connect to a building main supply electricity must pass The National Electric Code (NEC) ANSI/NFPA.</td>
</tr>
</tbody>
</table>

### GPR006: Reliability

<table>
<thead>
<tr>
<th>GPR006</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>GPR006-01</td>
<td>The system wide Mean Time Between Failures (MTBF) must be greater than 1000hrs over the system lifetime.</td>
</tr>
<tr>
<td>GPR006-02</td>
<td>Reliability inspection conducted over 24hrs without any obvious failure</td>
</tr>
<tr>
<td><strong>GPR007:</strong></td>
<td><strong>Maintainability</strong></td>
</tr>
<tr>
<td>GPR007-01</td>
<td>The system wide Mean Time To Repair (MTTR) must be less than 1 week over the system lifetime.</td>
</tr>
<tr>
<td>GPR007-02</td>
<td>Maintainability inspection performed</td>
</tr>
<tr>
<td><strong>GPR008:</strong></td>
<td><strong>Manufacturability</strong></td>
</tr>
<tr>
<td>GPR008-01</td>
<td>All production designs must be built from components and subassemblies that have a sustainable source of supply over the system lifetime.</td>
</tr>
<tr>
<td>GPR008-02</td>
<td>Each item on the BOM must have at least two suppliers.</td>
</tr>
<tr>
<td>GPR008-03</td>
<td>Analysis performed identifying any tolerance critical components and proves that the tolerances are adequate to meet system requirements at that yield.</td>
</tr>
<tr>
<td><strong>GPR009:</strong></td>
<td><strong>Life Cycle Sustainability</strong></td>
</tr>
<tr>
<td>GPR009-01</td>
<td>Production designs evaluated according to a generally recognized global sustainability metric or index such as a Life Cycle Assessment (LCA)</td>
</tr>
<tr>
<td>GPR009-02</td>
<td>Sustainability report demonstrating the degree to which the design is sustainable</td>
</tr>
<tr>
<td><strong>GPR010:</strong></td>
<td><strong>Ethics Report</strong></td>
</tr>
<tr>
<td>GPR010-01</td>
<td>The project must be evaluated with respect to explicit ethical principles, particularly the IEEE Code of Ethics.</td>
</tr>
<tr>
<td>GPR010-02</td>
<td>Format, style, and methodology of the ethics report shall be in accordance with standards established by Lafayette College course ES225.</td>
</tr>
<tr>
<td><strong>GPR011:</strong></td>
<td><strong>Project Demonstration</strong></td>
</tr>
<tr>
<td>GPR011-01</td>
<td>Unattended display offering a self-contained, active demonstration that would excite the interest of students, faculty, and ECE Department visitors</td>
</tr>
<tr>
<td>GPR011-02</td>
<td>The demo must fit in a compact public area and operate safely without unreasonable disturbance of its neighbors.</td>
</tr>
<tr>
<td>GPR011-03</td>
<td>If activated, the demo must shut itself down after a set amount of time.</td>
</tr>
<tr>
<td>GPR011-04</td>
<td>The MTTR and MTBF of the demo must meet or exceed the project-level Maintainability and Reliability requirements.</td>
</tr>
<tr>
<td><strong>GPR012:</strong></td>
<td><strong>Final Disposal of Projects</strong></td>
</tr>
<tr>
<td>GPR012-01</td>
<td>If project is to be stored, materials should be in sealed container, locked cabinet, or secure room that contains only these materials from one project and no other.</td>
</tr>
<tr>
<td>GPR012-02</td>
<td>Portions of the project that are discarded must be done so in accordance with the Hazmat procedures.</td>
</tr>
<tr>
<td>GPR012-03</td>
<td>Paper documents that have been scanned per GPR002 shall be placed in a paper recycling bin.</td>
</tr>
<tr>
<td>GPR012-04</td>
<td>The project web site must be updated with all final documents that match the delivered system. Obsolete documents shall be removed.</td>
</tr>
</tbody>
</table>
3.0 **Subsystem Evaluation**

For inspection, analysis, and testing of individual subsystems, refer to the appropriate Quality Assurance Report. QA Reports for the RPI, ESS, FIB, SC, and SCADA can be found at the project website, http://sites.lafayette.edu/ece492-sp10/.

4.0 **System Evaluation**

The first step in evaluating the system is DC Load Integration, which involves running the system with a DC Load in place of the FIB and AC Load. In Low Voltage DC Load Integration, the ESS is run in Low Voltage Mode (it is wired so that only some of the batteries are used; the rest are bypassed) and a low-voltage DC Source is used in place of the photovoltaic array. In High Voltage DC Load Integration, the ESS is run in normal high voltage mode (with all battery cells connected in series) and a high-voltage DC source is used in place of the photovoltaic array. In Photovoltaic DC Load Integration, the ESS is run in normal mode and the PV array is used to provide power to the RPI—PV DC Load Integration is integration of everything in the system except the FIB.
4.1 System Checkup

4.1.1 Basic Functionality Test

*Preconditions:*

1. The system is off.
2. Make sure the ESS is charged to over the 55% threshold.
3. From the full integrated system, disconnect the FIB from the system and add the DC source and DC load for testing (see Figure 2).

![Figure 2: Basic Functionality Test Block Diagram](image-url)
LPRDS Operation States

**Off**
- Safety Loop Open
- No LVDC
- FitPC off
- PVHV off
- ESSHV off

**Booting**
- Safety Loop Open
- LVDC
- FitPC booting
- Start all software
- PVHV off
- ESSHV off

**Shutdown**
- Safety Loop Open
- LVDC
- FitPC off
- PVHV off
- ESSHV off

**LV Standby Unsafe**
- Safety Loop Open
- LVDC
- FitPC running
- PVHV off
- ESSHV off

**LV Standby Safe**
- Safety Loop Closed
- LVDC
- FitPC running
- PVHV off
- ESSHV off

**HV Unsafe**
- Safety Loop Open
- LVDC
- FitPC
- PVHV on
- ESSHV on

**HV Standby**
- Safety Loop Closed
- LVDC
- FitPC
- PVHV on
- ESSHV on

**Operational**
- Safety Loop Closed
- App Control
- LVDC
- FitPC
- PVHV on
- ESSHV on

---

**Potential LV Faults**
- Ground Fault
- Max temp exceeded
- Over Voltage
- Under Voltage
- Over Current

**Potential HV Faults**
- Ground Fault
- Loss of ESSHV

---

*Figure 3: System State Diagram*
Test:

*Note: The PicoLCD will display the current system state.

<table>
<thead>
<tr>
<th>#</th>
<th>Simple Diagram</th>
<th>Input</th>
<th>Passing Criteria</th>
<th>P/F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Provide LV to power the FIT PC.</td>
<td>System enters Booting state.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Use DC source to simulate presence of HV from PV array</td>
<td>System enters HV Unsafe state.</td>
<td></td>
</tr>
<tr>
<td></td>
<td><img src="image1.png" alt="Diagram" /></td>
<td>Alarm goes off. Button silences alarm.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>From the HV Unsafe state, attempt the following:</td>
<td>System stays in HV Unsafe state.</td>
<td></td>
</tr>
<tr>
<td></td>
<td><img src="image2.png" alt="Diagram" /></td>
<td>1: Start Batt Mgmt App</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2: Trigger a fault by pushing the button on the side of</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>the tower.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3: Clear a fault in the RPI</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>For 1 only: An error message is displayed in terminal.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Action</td>
<td>Result</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>------------------------------------------------------------------------</td>
<td>------------------------------------------------------------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Manually disconnect simulated PV HV and confirm with HV Disconnect App.</td>
<td>System enters LV Standby Unsafe state.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Must confirm proper HV detected.</td>
<td>HV detected properly:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RPI input:</td>
<td>____________________________</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RPI out/SC in:</td>
<td>____________________________</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ESS/SC:</td>
<td>____________________________</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SC out/FIB in:</td>
<td>____________________________</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FIB output:</td>
<td>____________________________</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Start Batt Mgmt App</td>
<td>System stays in LV Standby Unsafe state.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Manually reconnect simulated PV HV</td>
<td>System enters HV Unsafe state.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Alarm goes off.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Shut down and restart the system.</td>
<td>System enters HV Unsafe state.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>From the Booting state, use DC source to simulate presence of HV from ESS</td>
<td>Alarm goes off.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td><img src="image" alt="Diagram" /></td>
<td>Manually disconnect simulated ESS HV and confirm with HV Disconnect App. From LV Standby Unsafe state, manually reconnect simulated ESS HV.</td>
<td>System enters HV Unsafe state and remains in that state. Alarm goes off.</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td><img src="image" alt="Diagram" /></td>
<td>Shut down and restart the system. From the Booting state, trip the safety loop.</td>
<td>System enters LV Standby Unsafe state</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td><img src="image" alt="Diagram" /></td>
<td>Clear faults in the RPI</td>
<td>System enters LV Standby Safe state</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td><img src="image" alt="Diagram" /></td>
<td>Start Batt Mgmt App</td>
<td>System stays in LV Standby Safe state. An error message is displayed in terminal</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td><img src="image" alt="Diagram" /></td>
<td>From the LV Standby Safe state, check safety loop operation by pushing the shutdown button on outside of tower.</td>
<td>System enters LV Standby Unsafe state. Alarm goes off.</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Description</td>
<td>Expected Outcome</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>-------------</td>
<td>------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Return to the LV Standby Safe state. Check safety loop operation by disconnecting a safety cable.</td>
<td>System enters LV Standby Unsafe state. Alarm goes off.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Return to the LV Standby Safe state. Shut down the FIT PC.</td>
<td>System enters Shutdown state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Remove LV</td>
<td>System enters Off state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Return to Shutdown state. Restart the FIT PC.</td>
<td>System enters Booting state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Return to the LV Standby Safe state. Use a DC source to simulate the presence of HV from the ESS, then add a DC source to simulate the presence of HV from the PV array.</td>
<td>System enters HV Standby state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>While in HV Standby state, trigger a fault by removing the simulated ESS HV.</td>
<td>System enters HV Unsafe state Alarm goes off.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Return to HV Standby State. Enter SW command to run the Batt Mgmt App</td>
<td>System enters Operational state</td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>Enter SW command to stop Batt Mgmt App</td>
<td>System enters HV Standby state</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>Return to Operational state. Trigger a fault by pushing the button on the side of the tower</td>
<td>System enters HV Unsafe state. Alarm goes off.</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.1.2 Reliability and Maintainability Test

**Preconditions:**

1. The system is off.
2. From the full integrated system, disconnect the FIB from the system and add the DC source and DC load for testing (see Figure 2).

**Test:**

Bring the system to Operational State. Run the Batt Mgmt App and allow the system to run for 24 consecutive hours.

**Passing Criteria:**

a. The system runs for 24 hours without unexpected faults or failures
b. No ambient temperatures are read above 40°C

| T in RPI: __________ | T in FIB: __________ |
| T in ESS: __________ | T in SC: __________ |
4.2 Low Voltage Testing

4.2.1 Low Voltage DC Load Integration Battery Management Test

This test forces the system through all states of the SC Algorithm at low voltage. The system is connected as shown in Figure 4. In DC Load Integration, the output of the SC is disconnected from the input to the FIB and connected instead to a DC Load. For this test, a low-voltage DC voltage source is used in place of the PV array so that the test can be conducted at any time. Also, the ESS is replaced with a low-voltage DC source, which allows the test to be run faster because the tester can simulate the ESS voltage instead of waiting for the ESS to charge and discharge to the appropriate levels. Voltage thresholds are scaled for low-voltage operation.

Preconditions:

1. The system is off.
2. Ensure that the Battery Management App. is programmed for LV thresholds.
3. From the DC Load Integrated system, remove the HV cable between ESS and SC and connect the DC source to the SC (see Figure 4).

---

*Figure 4: LV DC Load Integration Battery Management Test*
Figure 5: SC State Transition Diagram
**Test:**

*Note: The terminal will display the current SC state.*

Bring the system to the Operational state. Then:

<table>
<thead>
<tr>
<th>#</th>
<th>Input</th>
<th>Passing Criteria</th>
<th>P/F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enter the command to run the Battery Management Application. Observe switch operation through the clear covering of the SC.</td>
<td>The SC enters S1, then S2 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>While in S2, increase the simulated ESS voltage to $\geq 100%$</td>
<td>The SC enters S4 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transition Voltage: _______________</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>While in S4, decrease the simulated ESS voltage to $\leq 20%$</td>
<td>The SC enters S2 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transition Voltage: _______________</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>While in S2, increase the simulated ESS voltage to between 55% and 100%</td>
<td>The SC enters S3b in the next cycle.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transition Voltage: _______________</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>While in S3, increase the simulated ESS voltage to $\geq 100%$</td>
<td>The SC enters S4 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transition Voltage: _______________</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>While in S4, shut down and restart the Batt Mgmt App</td>
<td>On restart, the SC enters S1, then S4 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>While in S4, decrease the simulated ESS voltage to between 20% and 65%</td>
<td>The SC enters S3b in the next cycle.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transition Voltage: _______________</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>While in S3, shut down and restart the Batt Mgmt App</td>
<td>On restart, the SC enters S1, then S3a in the next cycle, then S3b the next.</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>While in S3, decrease the simulated ESS voltage to $\leq 20%$</td>
<td>The SC enters S2 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transition Voltage: _______________</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Result</td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>-----------------------------------------------------------------------------------------------</td>
<td>--------------------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>While in S2, shut down and restart the Batt Mgmt App</td>
<td>On restart, the SC enters S1, then S2 in the next cycle</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>While in S2, simulate a fault: trigger a ground fault by connecting a 40kOhm resistor from RPI HV to ground</td>
<td>The SC enters SF in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>While in SF, clear the fault in the RPI</td>
<td>The SC enters S1 in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>While in S3, simulate a fault: trigger a ground fault by connecting a 40kOhm resistor from RPI HV to ground</td>
<td>The SC enters SF in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>While in S4, simulate a fault: trigger a ground fault by connecting a 40kOhm resistor from RPI HV to ground</td>
<td>The SC enters SF in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>While in S1, trigger a ground fault by connecting a 40kOhm resistor from RPI HV to ground</td>
<td>The SC enters SF in the next cycle.</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>Alarm goes off every time system enters SF</td>
<td></td>
</tr>
</tbody>
</table>
4.2.2 Low Voltage AC Production Test

This test verifies that the FIB produces a scaled AC output at low voltage. The system is connected as shown in Figure 6. The ESS is run in Low Voltage Mode, and a low-voltage DC voltage source is used in place of the PV array so the test can be run at any time. Voltage thresholds are scaled for low-voltage operation.

Preconditions:

1. The system is off.
2. Ensure that the Battery Management App. is programmed for LV thresholds.
3. From the fully integrated system, connect the output of the transformer to an AC load (see Figure 6).
Test:

Bring the system to the Operational state, then run the Battery Management Application.

Passing Criteria:

<table>
<thead>
<tr>
<th></th>
<th>Required Value</th>
<th>Measured Value</th>
<th>P/F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>120V RMS ± 10V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>≤ 10A RMS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>60Hz (± 0.03Hz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient Overshoot</td>
<td>&lt; 5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2% Settling Time</td>
<td>&lt; 33ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Steady-State Error</td>
<td>&lt; 3%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>&lt; 3%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.2.3 Low Voltage AC Load Test

This test verifies that the system can run an AC load at low voltage. A low-voltage DC source is used to power the system so the test can be run at any time. The system is connected to an AC load.

**Preconditions:**

1. The system is off.
2. Ensure that the Battery Management App. is programmed for LV thresholds.
3. From the fully integrated system, connect the output of the transformer to an AC load (see Figure 7).

![Figure 7: LV AC Load Block Diagram]

**Test:**

Bring the system to the Operational state, then run the Battery Management Application.

**Passing Criteria:**

A simple AC load will be run (e.g. a light bulb will illuminate).
4.3 High Voltage Testing

4.3.1 High Voltage DC Load Integration: Battery Management Test

This test forces the system through all states of the SC Algorithm at high voltage. The system is connected as shown in Figure X. In DC Load Integration, the output of the SC is disconnected from the input to the FIB and connected instead to a DC Load. For this test, a high-voltage DC voltage source is used in place of the PV array so that the test can be conducted at any time. Also, the ESS is replaced with a high-voltage DC source, which allows the test to be run faster because the tester can simulate the ESS voltage instead of waiting for the ESS to charge and discharge to the appropriate levels. Voltage thresholds are scaled for high-voltage operation.

4.3.2 High Voltage AC Production Test

This test verifies that the FIB produces the correct AC output at high voltage. The system is connected as shown in Figure X. The ESS is run in High Voltage Mode, and a high-voltage DC voltage source is used in place of the PV array so the test can be run at any time. Voltage thresholds are scaled for high-voltage operation.

4.3.3 High Voltage AC Load Test

This test verifies that the system can run an AC load at high voltage. A high-voltage DC source is used to power the system so the test can be run at any time. The system is connected to an AC load.

4.4 PV Integration

4.4.1 PV DC Load Integration: Battery Management Test

This test forces the system through all states of the SC Algorithm at high voltage. The system is connected as shown in Figure X. In DC Load Integration, the output of the SC is disconnected from the input to the FIB and connected instead to a DC Load. For this test, the PV array provides power to the RPI. The ESS is replaced with a high-voltage DC source, which allows the test to be run faster because the tester can simulate the ESS voltage instead of waiting for the ESS to charge and discharge to the appropriate levels. Voltage thresholds are scaled for high-voltage operation.

4.4.2 PV AC Production Test

This test verifies that the FIB produces the correct AC output at high voltage. The system is connected as shown in Figure X. The ESS is run in High Voltage Mode, and the PV array provides power to the RPI. Voltage thresholds are scaled for high-voltage operation.

4.4.3 PV AC Load Test

This test verifies that the system can run an AC load at high voltage. The PV array provides power to the RPI, and the system is connected to an AC load.
5.0 **Acceptance Test Report**

The Acceptance Test Report documents system testing, including analysis of any failures, corrective action taken, and continuation of testing once a problem has been corrected.

5.1 **Testing**

5.1.1 **Basic Functionality Test**

<table>
<thead>
<tr>
<th>#</th>
<th><strong>Passing Criteria</strong></th>
<th><strong>Observation</strong></th>
<th><strong>P/F</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>System enters Booting state.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>System enters HV Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>System stays in HV Unsafe state for each attempt. For (1), an error message is displayed in terminal.</td>
<td>1: Start App 2: Fault button 3: Clear fault</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>System enters LV Standby Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HV detected properly:</td>
<td>RPI input:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>RPI out/SC in:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ESS/SC:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SC out/FIB in:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FIB output:</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>System stays in LV Standby Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>System enters HV Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>System enters HV Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>System enters HV Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>System enters LV Standby Unsafe state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>System enters LV Standby Safe state</td>
<td>Clear faults in the RPI</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>System stays in LV Standby Safe state and an error message is displayed in terminal</td>
<td>Start Batt Mgmt App</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>System enters LV Standby Unsafe state. Safety loop opens All subsystems disconnect outside HV terminals All subsystems enter fault state SCADA alarm is audible</td>
<td>From the LV Standby Safe state, check safety loop operation by pushing the shutdown button on outside of tower.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>System enters LV Standby Unsafe state</td>
<td>Return to the LV Standby Safe state. Check safety loop operation by disconnecting a safety cable.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Safety loop opens</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>All subsystems disconnect outside HV terminals</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>All subsystems enter fault state</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SCADA alarm sounds</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Button quiets alarm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>System enters Shutdown state</td>
<td>Return to the LV Standby Safe state. Shut down the FIT PC.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>System enters Off state</td>
<td>Remove LV</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>System enters Booting state</td>
<td>Return to Shutdown state. Restart the FIT PC.</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>System enters HV Standby state</td>
<td>Return to the LV Standby Safe state. Use a DC source to simulate the presence of HV from the ESS, then add a DC source to simulate the presence of HV from the PV array.</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>System enters HV Unsafe state</td>
<td>While in HV Standby state, trigger a fault by removing the simulated ESS HV.</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>System enters Operational state</td>
<td>Return to HV Standby State. Enter SW command to run the Batt Mgmt App</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>System enters HV Standby state</td>
<td>Enter SW command to stop Batt Mgmt App</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>System enters HV Unsafe state</td>
<td>Return to Operational state. Trigger a fault by pushing the button on the side of the tower</td>
<td></td>
</tr>
</tbody>
</table>
5.1.2 Reliability and Maintainability Test
5.1.3 Low Voltage DC Load Integration Battery Management Test
5.1.4 Low Voltage AC Production Test
5.1.5 High Voltage DC Load Integration Battery Management Test
5.1.6 High Voltage AC Production Test
5.1.7 PV Battery Management Test
5.1.8 PV AC Production Test

5.2 Inspection and Analysis

4.2.1 Power Independence

4.2.2 Safety

Safety Interface

Safety and Good Practice

4.2.3 Reliability and Maintainability

4.2.4 Manufacturability and Life Cycle Sustainability

4.2.5 Project Materials

Environmental Concerns

Electromechanical Interference / Electromagnetic Compatibility

Hazardous Materials

Disposal of Project Materials

4.2.6 Documentation